PowerArti$^\text{™}$-XP
Analysis-driven Automatic RTL Power Reduction

PowerArti$^\text{™}$-XP is a complete RTL Design-For-Power (DFP™) environment with fully-integrated advanced analysis and automatic reduction. Utilizing a unique Analyze-Visualize-Reduce framework, PowerArti$^\text{™}$-XP delivers maximum power savings for complex SoCs and IPs with a tight control over design impact and downstream flow.

With a comprehensive set of power reduction techniques and a range of visual debug diagnostics, PowerArti$^\text{™}$-XP is the low power design tool for RTL engineers.

**Overview**

Power is the number one design criterion today and the designers are forced to produce RTL designs that are more power efficient and meet the power requirement demands. However, the current tools and methodologies are unable to systematically address power at the RTL due to the factors such as poor power visibility, limited reduction techniques and lack of power-smart automation.

PowerArti$^\text{™}$-XP addresses all of these concerns and enables designers to create power-efficient RTL. With proven power analysis, rich power reduction features and push button automation, PowerArti$^\text{™}$-XP is a complete RTL Design-For-Power (DFP™) environment with fully-integrated advanced analysis and automatic reduction. Utilizing a unique Analyze-Visualize-Reduce framework, PowerArti$^\text{™}$-XP delivers maximum power savings for complex SoCs and IPs with a tight control over design impact and downstream flow.

With a comprehensive set of power reduction techniques and a range of visual debug diagnostics, PowerArti$^\text{™}$-XP is the low power design tool for RTL engineers.

**KEY CAPABILITIES**

- Achieves predictable single-pass power savings with production-proven RTL power analysis
- Maximizes power savings with clock, memory and datapath power reduction techniques
- Allows automatic power-efficient RTL generation for trade-off of power vs. other application-specific design constraints
- Guides clock gating synthesis for higher power savings and better skew control
- Delivers rapid power debug with a powerful yet intuitive graphical cockpit and user-programmable interface based on the Open Access database (OADB)
- Runs million gate-equivalent RTL in minutes

**Production-proven Full-chip RTL Power Analysis**

PowerArti$^\text{™}$-XP offers the performance and breadth of algorithms needed to handle true full-chip RTL power analysis, even for multi-million gate designs. Fast yet accurate and comprehensive power analysis allows designers to pinpoint power problems early in the design flow. PowerArti$^\text{™}$-XP is able to efficiently analyze designs with multiple power supplies, mixed Verilog-Verilog2001-VHDL
descriptions and embedded IP models. PowerArtist-XP also works at the gate level, where it can be used both for post-synthesis, as well as post-layout power analysis with full SPEF backannotation.

Automatic Analysis-Driven RTL Power Reduction

PowerArtist-XP reduction is driven by Apache’s industry standard RTL power analysis technology. Timing-aware RTL power analysis algorithms provide early access to power with proven correlation to gate-level power. This unique capability provides predictable power reduction and eliminates unnecessary iterations between RTL, synthesis, and physical design. Power reduction choices are quickly evaluated at RTL before synthesis, for various trade-off conditions. As a result, designers are able to achieve maximum power reduction with minimum RTL edits and focus on the highest power saving opportunities.

PowerArtist-XP’s analysis-driven reduction enables intelligent design decisions – for maximum power savings, with minimum design impact

Peak Power and Power vs. Time Analysis

PowerArtist-XP allows user to define modes of operation (e.g. active, standby, idle, sleep, scan, reset) and monitors each mode and its related power consumption. Time-based power at RTL enables power profiling at user-defined time intervals down to the logic simulation resolution. By providing visualization of where peak power is consumed, PowerArtist-XP addresses issues such as power bus sizing, electromigration analysis and power supply requirements prior to synthesis.

Design Activity Analysis

PowerArtist-XP vector analysis capability enables designers to visualize activity for an entire test suite, for any combination of modules in the design, quickly identifying coverage problems and unexercised power modes. Throughout the design process, vector analysis can be used to visualize the activity in multiple hierarchical blocks to make sure the test suite covers the high power modes of operation, and selects small, power intensive time slices for detailed power verification. Using the vector analysis capability, designers can easily identify vector sets that do not have adequate activity to perform meaningful power analysis. Vector analysis can also identify vectors that may cause di/dt or electromigration issues, and aid designers in selecting critical vector sets for more detailed analysis.

eXpert Power Reduction Technology

PowerArtist-XP’s eXpert Power Reduction Technology (XPRT) is a comprehensive set of power reduction techniques delivering significant power savings. XPRT targets power reduction opportunities in clock, memory and datapath sections that are complementary to synthesis. It has a wide range of clock power reduction techniques from combinational to sequential clock gating that apply at the register and block level. It generates synthesis constraints to prevent insertion of those clock gates that can increase power consumption resulting in higher power savings. These constraints can also be used to eliminate a large number of clock gates that do not save significant amount of power resulting in better clock skew control and less routing congestion. Memory power reduction techniques include redundant cycle elimination, memory gating, and memory splitting. Datapath power reduction techniques eliminate power due to wasteful activity in deep cones of logic. XPRT automatically generates power-efficient RTL and makes precise edits to preserve the original formatting.

‘What-if’ Power Protoyping

PowerArtist-XP enables the user to predict the effects at global SOC-level as well as downstream fine-grained power reduction techniques such as power gating (power shutoff, PSO), voltage islands (multiple supply voltages, MSV), clock gating, and multi-Vt optimizations. It can accept power
PowerArtist-XP Advantage

PowerArtist-XP employs a systemic approach to power reduction by delivering a complete RTL Design-For-Power methodology. With PowerArtist-XP, designers can:

• Understand the power profile of their designs in terms of hotspots, power bugs, power-inefficient modules and architectures

• Identify and visualize highest impact power reduction opportunities across the design, module and sub-module levels

• Control the automatic RTL rewrite to achieve maximum power savings with minimum RTL edits and minimum design impact

• Monitor power efficiency via regressions throughout the design flow

With a comprehensive set of features within the Analyze-Visualize-Reduce framework, PowerArtist-XP is the most comprehensive RTL Design-For-Power solution enabling maximum power savings, in minimum time and with minimum design impact.

Graphical Cockpit for RTL Power Visualization

PowerArtist-XP includes a powerful graphical cockpit for viewing, understanding and debugging power consumption and reduction. This tightly interlinked environment enables designers to perform customized activity and power-related queries quickly and easily. Designers can build power regressions to track the power-efficiency of their designs and locate power-erratic design changes between various RTL versions. The API access can also be used for interoperability with other third-party tools for low-power design.

OpenAccess Database API

PowerArtist-XP utilizes Si2’s OpenAccess standard database (OADB) and supports OpenAccess API for database searches. Use of OpenAccess and OADB scripts enables designers to perform customized activity formats such as CPF and UPF together with the RTL design description. The user can then change the design partitioning, power supplies, or clock gating directives and quickly re-analyze the design to monitor changes in power consumption. Once the design architecture is finalized, PowerArtist-XP can write out CPF or UPF directives for the downstream flow.

OADB API enables customer interactive queries – also possible in batch mode

PowerArtist-XP power analysis and debug environment
Features

**XPRT RTL POWER REDUCTION**
- Clock Gating: Block and register, combinational and sequential
- Memory redundant cycle elimination, clock gating, and splitting
- Datapath wasted activity elimination
- Modal power bug elimination

**RTL POWER ANALYSIS**
- Average and peak power, vectorless and vector-based
- Detailed power breakdown by mode and category
- Power stimulus management including identification of vectors critical for power and voltage drop
- What-if power prototyping
- Integration with leading High Level Synthesis tools enabling low-power ESL design

**GATE-LEVEL POWER SIGN-OFF**
- Using RTL simulations, gate-level simulations or vectorless

**POWERCANVAS RTL POWER VISUALIZATION**
- Integrated analysis plus reduction GUI
- Cockpit for driving interactive power reduction
- Searching, filtering and sorting multiple available power views

**INPUT**
- Design: Verilog, VHDL, System Verilog
- Simulation Vectors: VCD, FSDB, SAIF
- Library: Liberty (.lib)
- Power Formats: CPF, UPF
- Synopsys Design Constraints
- Parasitics: SPEF

**DATA MODEL**
- OpenAccess database
- OpenAccess API support

**OUTPUT**
- Detailed power reports and waveforms
- Power-efficient RTL
- Clock gating synthesis constraints
- Power formats: CPF, UPF

**PLATFORMS**
- Solaris, Linux (RHEL, SuSE)