SUBSTRATE NOISE FULL-CHIP LEVEL ANALYSIS FLOW FROM EARLY DESIGN STAGES TILL TAPEOUT

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Agenda

• Introduction
  – Technology and ASIC Trends
  – Traditional Approach for Substrate Noise Analysis

• Background
  – Substrate noise
  – Substrate Noise Analysis

• Early Analysis and Substrate Noise Analysis Flow
  – Inputs
  – Concept
  – Flow
  – Examples

• Flow Application Examples

• Correlation

• Summary
Technology Trends
ASIC Trends

- SoCs incorporate RF, Analogue and digital IPs
- Frequencies increase
- Chip dimensions decrease
  - Increase of generated noise
  - Increase of victims sensitivity
  - Reduced isolation between the two

Rise of substrate noise risks
Traditional Approach for Substrate Noise Analysis

- Relies on final chip design database
- Occurs during the last stages prior to tapeout
- Used for signoff, lessons for next projects or informational purposes

Required: A method to analyze substrate noise earlier
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Switching Noise’s Propagation Paths
The switching activity involves current consumption and generates voltage variations.

Local activity propagates noise within the entire SoC:
1. Through the Power and Ground Metal Grid
2. Through the Package
3. Through the Substrate layers

Substrate Noise results from a combination of SoC PDN, Package and Substrate Network
Many designs use a Triple-Well CMOS process, i.e. N-well, P-well and deep N-well.

The Substrate RC network is extracted according to the foundry process description:

- Same type wells connect resistively
- Opposite type wells connect through coupling (surface or side)

Thick layers can be decomposed into multiple thicknesses to improve resolution.
Substrate Noise Analysis – SignOff Flow

**Data Inputs**
- SoC data
  - LEF
  - DEF
  - SPEF
  - GDSS
- Package data
  - layout db
  - pre-extracted model
- Activity data
  - VCD based
  - Vectorless + STA
- Library data
  - Current profiles
  - Intrinsic parasitics
- Technology rules

**Noise Simulation**
- **1-** Data Import & Setup
- **2-** P/G Grid & Substrate Extraction
- **3-** Power Calculation
- **4-** Dynamic Simulation

**Results Exploration**
- Simulation vs. Measurements
- Voltage Amplitude per Layer
- Substrate Weakness Map
- Point to Point Resistance & Tracing

**RedHawk / Totem**

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A page from a presentation slide at DesignCon 2015, showing a flowchart for substrate noise analysis, with detailed steps and relevant tools.
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  – Chip level analysis inputs
  – Early analysis concept
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In order to analyze full-chip top level substrate noise, following information is required:

- **VLSI**
  - Netlist, Activity, Timing

- **Backend**
  - Chip dimensions, Floorplan, Layout of digital blocks, I/O ring, power network, parasitics

- **Analogue/RF**
  - Layout of Analogue/RF blocks, activity

- **Packaging**
  - Connectivity, parasitics

- Some of this information is ready earlier than the complete PNR database
- Some of this information can be evaluated based on past experience
Early Analysis Concept

Analyze substrate noise on an **emulated** database, generated from available information, experience and assessments

**Early analysis on initial data**

**Final analysis on complete design**

Interim analysis 2 on developing data

Interim analysis 3 on developing data

Required: A flow of work to match abilities and needs
Substrate Noise Analysis Flow

• Placing the inputs on a timeline according to plan
• schedule can split by input’s intended usage:
  – Noise generation
  – Noise propagation
• The project’s schedule dictates data availability
• The phases are set according to needs
• Begins early in the design stages
• Defined by the inputs and setup used
• Inputs split between noise generation and noise propagation
• Integrates into the design stages
• Flexible
Flow Example: Design Updates - Pad Locations

The amount of supply pads was reduced.
Substrate noise analysis was required to evaluate the impact.

Original pad location

Reduced pad location
Flow Example: Noise Generation

Circuit Simulation of the Aggressor

Probe location

Aggressor

Victim

Victim (Deep NW)

Noise [v] vs. Time [ns]
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Flow Applications

- Substrate noise related fixes and design alternatives require changes in
  - Aggressor
  - Floorplan
  - Isolation
  - Layout
  - Activity

- Modifications in these design elements are costly

- Solution: Using the technique of the flow (emulated database)
  - Implementing alternative designs without modifying the real design
  - Evaluating the optional modifications
  - Validating expected trends
Flow Application Example: Aggressor

Comparing noise maps generated by injection at different locations:
A. Original location on the south wall
B. North west corner
C. Left side of the victim

Noise measured on the victim in each case
Comparing substrate noise between two floorplans:

- RF victim is on the north wall
- RF victim is on the east wall
Flow Application Example: Isolation - Guard-Bands

- Adding a guard-bands of P-diffusion and metals on either sides of the RF block
- The guard-bands are grounded
Flow Application Example: Isolation - Guard-Bands - Results

- Effects can be observed both inside and outside of the victim
- Alternative ring architectures may be easily implemented and compared

Noise Scale

Original design Noise map

Addition of side guard bands Noise map
Flow Application Example: Isolation - Deep N-Well

- Deep N-well is introduced under sensitive areas
- Dramatic effects can be observed in the modified areas
- Some occur in adjacent areas
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What about Predictability?

Prototyping Analysis
Relative comparisons between different implementation scenarios

Sign-Off Analysis
Correlation versus measurements

Noise Coupling Analysis for Advanced Mixed-Signal Automotive IC’s
DAC 2014, Jacob Bakker - NXP Semiconductors
Correlation: Prototyping vs. Final 1/2

Injected Noise:
- 1A Sinusoidal, 800MHz @ 3255, 582 Metal2

Nwell & Pwell Voltage Scale:
- **Red** V > 10mV
- **Purple** V < 1mV

Observations:
- Overall Noise attenuation is similar with some offset
- Differences reside within channels and in Memory cuts

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Nwell & Pwell Voltage Scale:
- **Red** V > 0.9mV for Proto or 1mV for Final
- **Purple** V < 0.1mV

Observations:
- Variations inside IP are very similar
- Offset is explained by impedance differences of the path between injection point and victim location
Correlation: Prototyping vs. Final 2/2

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<thead>
<tr>
<th>Prototype Analysis</th>
<th>Vmax</th>
<th>Peak-2-Peak</th>
<th>dbV</th>
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<td>Victim PW Probe A</td>
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<table>
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</tr>
</tbody>
</table>

Probes inside victim IP from Prototype db

Probes inside victim IP from Final db

PW’s Voltage Waveforms over time
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• Early Substrate analysis
  – Often required
  – Depends on input quality and design knowledge
  – Reliable based on correlation

• Flow
  – Accommodate to the project’s schedule
  – Flexible

• Method (emulated database)
  – “Cheap” evaluation of alternative designs
Thank you