Practical Considerations in Selection of 2.5D/3D Package Solutions

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Abstract

• Amidst the excitement of the emergence of 2.5D and 3D packaging solutions, each company must partner with customers, supply chain and tool providers to determine if the needs of the end product are best served by these new technologies versus single chip packaging, MCM or a combination of solutions. The presentation will consider the emerging landscapes from a High End Custom solution perspective and explore how the factors governing the decision making process will change over time as the tools, standards and supply chain matures.
3D TSV Packaging Market Value
2015 forecast / breakdown by application (in $M)

Yole Development ©
October 2009

3D TSV Packaging Market Value
2015 Forecast

TOT ~ $4.1B

- We forecast Logic + Memory applications to drive > 30% of the 3D TSV Packaging market value by 2015.
- CIS, MEMS, Sensors & HB-LED to drive ~30% following revenues
- Memory+Memory stacking (of DRAM, NAND) combined will drive ~ 20% of the market value
- Wireless SiP, Logic 3D-SOC/SiP, Power & Analog components will drive the last 20%
Key Motivators for Multi Die Package Solutions

• Latency
• Bandwidth
• Power
• Form factor
• Cost
Key Motivators for Multi Die Package Solutions

Latency and Bandwidth

- 40nm, 28nm High End Networking Silicon frequently exceeds 20mm per side.
- PCB ball pitch remains at 1mm.
- To support data caching connectivity (Bandwidth), package body sizes are exceeding 50mm per side.
- Latency issues compounded by increasing data rate and physical separation.
Key Motivators for Multi Die Package Solutions

Power

• In High End Networking Devices IO Switching typically consumes 20 - 40% of device power.

• Multi Die Packaging reduces IO power through
  • Reduced path length, capacitive loading
  • Ability to switch with reduced drive strength, lower voltage switching.
Key Motivators for Multi Die Package Solutions

Form Factor

• Reduced Form Factor, essentially replacing multiple packages on a board with a stack in a single package, significantly reduces board utilization and can shrink the overall end product.

• Reduced form factor enables new applications or products which were previously not possible
Key Motivators for Multi Die Package Solutions

Cost

• Multi die options configurations are typically more expensive than single package die options however overall cost of ownership may include board area or product size.

• Partitioning very large die has been modeled as cost effective and underlies Xilinx Virtex7 2000T strategy.
  – Javier DeLaCruz of eSilicon *estimated simple die partitioning to be cost effective at 18 – 24mm (varies by node)

• Mixing die from different technology nodes, different processes (Analog / Digital / Memory) and different suppliers may be cost effective through overall silicon cost, yield enhancement or NRE avoidance

* Reference EDA Interest Group 4/20/2011
Relative Connectivity Density

• The below chart shows the relative capability for single layer routing for different interconnect techniques for a 15mm Die. PCB density is shown for reference
  – PCB - 75u L/S
  – MCM - 18u L/S
  – “Advanced” MCM 5u L/S
  – 2.5D RDL at 2/3u L/S

• 3D stacking techniques can achieve significantly higher “single array routing” through array based TSV.
3DIC Tool-Box: Synthesis of Key Challenges

Wafer thinning technologies
- Grinding
- CMP
- Plasma
- Wet etching
- TSV nailing techniques

TSV formation
- TSV patterning
- TSV etching (low scalloping, low undercut)
- TSV isolation/seed/barrier: conformal and continuous deposition
- TSV filling: voidless deposition, CMP uniformity

Bonding / Assembly
- C2W and W2W bonding
- Inter-die connections (bumps, Copper pillars, etc.)
- Bonding materials & Underfill (pre-applied UF, CUF, WLUF...)

Wafer handling
- Temporary bonder/debonder
- Carrier wafer (glass / silicon)
- Temporary bonding materials

Dicing

+ Thermal Considerations, Silicon Design Tools, Keep out Zones for TSV, Routing Congestion etc
Why is 2.5D Attractive to early Adopters?

- Latency, Bandwidth, Power, Form Factor, Cost

And what does 2.5D leave on the table?
- Latency, Bandwidth, Power, Form Factor, Cost
Emerging Infrastructure

• Standards
  – Memory Configurations
    • JEDEC Wide I/O specification 512-bit memory interface at clock speeds to 266 MHz using SDR (single data rate) signaling. 17 Gbytes/sec at 1.2v
    • Micron HMC - 160 – 320 Gbytes/sec
  – Micro bump footprints

• Supply Chain
  – Interposer
  – Micro bumped Products

• KGD, self testing strategies

• Assembly Infrastructure
  – OSAT versus Foundry

• Opto Electronic Converters