Worst Case Switching Pattern for Core Noise Analysis

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Abstract
This paper demonstrates an optimum methodology to capture the worst case switching activity when performing the power integrity analysis for the core power of ASIC. The key approach is to capture the resonant frequency of the complete power delivery network (PDN), including the chip, package and board. From the FFT of the switching activity, the worst case pattern can be obtained by identifying the major frequency content which coincides with the resonance frequency of the PDN. The feasible process flow is demonstrated through an ASIC design. The results illustrate the interaction between the switching activity and the design of chip/package/board.

Authors Biography
Wheling Cheng received her Bachelor degree from Department of Electronics in Chiao-Tung University, Taiwan, and Ph.D. in 1995 from Department of Material Science and Engineering in Stanford University. In 1995 - 1997, she worked for nChip on multi-chip module development and fabrication. In 1997-1999, she worked for LSI Logic on the signal integrity analysis and package design. Since 1999, she has been working for Cisco Systems on the signal integrity and power integrity analysis. Her interests are 3D-modeling of high-speed interconnect and SERDES channel analysis.

Aveek Sarkar is Vice President of Product Engineering and Customer Support at Apache Design Solutions. Prior to joining Apache, Aveek held engineering positions at Sun Microsystems, Cadence, and National Semiconductor Corp. He holds a B.Tech from the Indian Institute of Technology, Kanpur, a MSEE from Oregon State University, and a MBA from Santa Clara University.

Shen Lin is Chief Technology Officer of Apache Design Solutions and a co-founder. Before founding Apache, Dr. Lin worked at Palo Alto HP Labs, focusing on inductance related signal integrity issues and contributing to the HP-Intel IA64 micro-processor design. In 2000, he co-authored a widely read book on state-of-the-art methods for interconnect titled "Interconnect Analysis and Synthesis", published by John Wiley & Sons. Prior to his work at HP Labs, Dr. Lin worked at LSI Logic developing on-the-fly ASIC design methodologies. His career began as a research staff member of the IBM T. J. Watson Research Center in Yorktown Heights, New York. Dr. Lin received his Ph.D. in EECS from the University of California, Berkeley in 1992, where he published his well-known thesis on recursive convolution for circuit simulation.

Ji Zheng is currently Director of Engineering at Apache Design Solutions, responsible for the development of the IC-Package-PCB co-analysis solutions for power, signal, and thermal integrity. Before Joining Apache in 2005, he worked for Sigrit Inc, Santa Clara, CA as Senior Technical Staff and R&D manager, responsible for development of package and PCB extraction and modeling tools, which have been widely adopted by the SI community. Ji Zheng earned his Ph.D. in Electrical Engineering from Shanghai Jiao Tong University and conducted his post-doctoral research in Oregon State University where his research focus was on the modeling of CMOS interconnects. He is a Senior Member of IEEE.
**Introduction**

In the ASIC design flow, power integrity analysis is required to ensure that enough decoupling capacitance is included in the silicon, on the package, and on the printed circuit board (PCB). In power integrity simulation, it is required to model the complete power delivery network (PDN), as well as the switching activity. Currently, no methodology exists for identifying the worst case switching for power integrity analysis. In some cases, it is assumed that the worst case power may be used to predict the worst case noise. In this presentation, examples will be given to demonstrate that the switching pattern for worst case power estimation may not be the same for worst case core noise prediction. In fact, core noise may be underestimated when the worst case power is assumed in the power integrity analysis.

**Background**

Power integrity analysis usually starts with the plot of impedance profile of the PDN, including the on-die decoupling capacitance, package structure, and the PCB decoupling scheme. The complete power impedance seen by the silicon usually resonates at around a few hundreds of Mega-Hertz (MHz). In Figure 1, one example of typical impedance profile of a PDN is shown with resonance frequency of 125MHz.

![AC impedance looking into the PDN](image)

*Figure 1: The typical AC impedance looking into the power delivery network*

To ensure the whole PDN is properly designed, transient analysis is usually performed to monitor the voltage noise. Based on the specified noise requirements at given locations, the simulated noise can be used to determine if sufficient decoupling capacitances have been included within the whole PDN. As shown in Figure 2, the analysis should include the current signature to mimic the switching activities of the silicon, as well as the models for the PDN, including the on-die decoupling capacitance, package structure, and the PCB decoupling scheme. While the PDN model can be obtained by using extraction tools, the current signature is dependent of the functions and the operation modes of the silicon. Thus, current signature may not be unique. In the following session, it will be
demonstrated that the current signature can dramatically influence the voltage noise prediction.

**Transient Analysis:**

**Noise Analysis with the typical current profile**

![Current Signature](image1.png)

![Noise Monitored](image2.png)

Interaction between the switching and the PDN impedance

To highlight the interaction between the resonant frequency of the PDN and a major component of the switching current, simulations were run with four experimental switching activities as shown in Figure 3. The PDN in the transient analysis has the resonance frequency of 125 MHz, as shown in Figure 1. Among the four switching cases, the first case has the exact 125 MHz switching frequency and has the lowest power. The second case has the 250 MHz switching frequency, and its power is the highest. The third and the four cases have the same 125 MHz switching pattern as the first case, plus some additional activities between the main 125 MHz activities.

**Figure 3: Four current profiles to illustrate the interaction with PDN**

**Which is the worst current profile for PI?**

![Current Profiles](image3.png)
Before the simulations were performed, the second case may appear to have more switching activities, and hence may generate more noise. However, the simulations predicted that the second case has the least noise. As summarized in Figure 4, each case is listed with the magnitude of the 125 MHz component, the average power, and the voltage range. In conclusion, the worst case noise occurs when the switching activity has major frequency components that coincide with the resonance frequency of the PDN, which is 125 MHz in this case. Note that the worst case power does not produce the worst case noise.

**Worst case current profile:**

<table>
<thead>
<tr>
<th>Major components matching package resonance frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>125 MHz component</td>
</tr>
<tr>
<td>Average Power</td>
</tr>
<tr>
<td>Voltage Range</td>
</tr>
</tbody>
</table>

Figure 4: Summarized results for the four experimental switching activities

It is concluded that for any given sets of switching activities, the worst case noise can be identified by performing FFT. The worst case noise should have the maximum magnitude of the frequency component that matches with the resonance frequency of the PDN. With this methodology, the true worst case switching activity can be captured in simulation and ensure that the sufficient amount of decoupling capacitance is included within the PDN for a given design. This approach is especially valuable for validating the package and PCB design. Furthermore, the worst case switching activity will be better understood, and hopefully will be avoided through the design.

The above four experimental switching activities have illustrated the interactions between the resonant frequency of the PDN and the major frequency component of the switching activity. The next step is to generate the worst case switching activity which comes from the real operation of a chip design. The methodology will have a profound impact as the resonant frequency of a PDN may accidentally match the major components of the switching current, and therefore, cause severe power noise. Thus, it is needed to have a tool which can automatically capture the worst case.

**Experimental Technique**

To validate the proposed methodology, simulations were performed on an ASIC using the RedHawk™ and Chip Power Model (CPM™) technologies from Apache Design.
Solutions. RedHawk is a commercially available dynamic power noise analysis tool that can perform cell level static and dynamic voltage drop analysis in Vector and VectorLess modes. These tools are used because they can generate the switching current profile which matches with the ASIC functional activities. Thus, the predicted worst case current profile would have the possibility of occurrence. From the worst case analysis results, one can identify potential areas of concern with the PDN, either on a local scale (high drop in a particular cell row) or on a global scale (large voltage swing at the BGA and/or package ports). In case any potential problem is identified through simulations, the designers would have the chance to improve the overall quality of the power delivery network. The ultimate goal is to prevent chip failures from happening due to power noise issues.

Technology Overview for Dynamic Analysis

Figure 5 illustrates various components in the PDN that need to be addressed in formulating the dynamic voltage noise. On the die side, the input data requirements can be broken down into two broad categories: design data and library data. The design data defines where different cells are placed, how the on-die power and ground routing are done (width, pitch, orientation, utilization), and how the cells are connected to these power and ground routing. Additional requirements include the loading information (signal and gate pin capacitance) for every cell and timing information like operating frequency (for different modes), input pin transition times (rising, falling) and the switching timing windows. Not all of the data is absolutely required for the analysis, but will add to the accuracy of the simulation. The design data can be provided either in DEF or GDS formats.

On the library side, the data present in the .lib (Liberty format) and the LEF, which provides electrical and physical properties for each cell are used. Memories, I/Os, custom logic, and standard cells that capture, among other electrical parameters, their switching current, intrinsic capacitances and effective series resistance are properly modeled. These
models are typically generated for each library at various process, operating voltage, and temperature (PVT) conditions and provide the input data required for a rigorous SPICE-like transient simulation of the power and ground network’s switching current at the block or full-chip level.

Once the design and library data are read in the power and ground network RLC model is extracted for the on-die P/G mesh network. This on-die P/G mesh network is connected to a package model (S-parameter or RLCK) on one side and the equivalent model of the cells on the other. A user provided VCD (RTL and gate-level VCD/FSDB data) or the VectorLess technology will identify the cells that will switch during the simulation and their switching states. The timing data is used to determine what time each cell will switch for each operating state. The cell models define how much current, capacitance and resistance each cell will offer for each switching cell. Once the P/G model is formulated, a true SPICE-like transient analysis is performed at a default time-step of 10ps to provide time domain voltage and current data at various parts of the design. Using pre-characterized models for every cell avoids the capacity limitations of SPICE but still provide SPICE-like simulation capabilities for the largest of designs. This approach using RedHawk have been correlated to silicon measurements in prior studies [1].

**Technology Overview of Chip Power Model**

From a dynamic analysis, a Chip Power Model (CPM) can be written out. The CPM technology should operate on the dynamic analysis database to generate reduced models of the chip power delivery network in SPICE compatible format. It should capture the switching current and parasitic components (RLC) associated with the on-die PDN. A vastly reduced SPICE netlist of an accurate electrical representation of multi-million instance designs enables quick but accurate package and board level AC, DC, and transient analyses for power delivery design. The current profile in the CPM can be created using either a VCD file (user provided vector) or by using a Vectorless approach. The VCD provides the dynamic analysis engine a switching scenario for the design. But if a VCD is not available, then a Vectorless engine is used to create a switching scenario.

A Chip Power Model represents the power and ground network of the chip with ports created at the bumps (for flip chip designs) and pads (for wire-bond designs). A CPM needs to determine the manner in which the ports connecting the die to the package are created. For a wire-bond design, each power and ground pad act as a port for the SPICE netlist. For a flip-chip design, having a port at every bump location is cumbersome and complex for subsequent simulations with package and board netlists. However, if one lumps all the power bumps into one port the subsequent model will not capture the distributed nature of the switching current and capacitance in a chip. To bypass the issues associated with the prior two models, one can partition a design into multiple regions each containing multiple power and ground bumps. This “grouping approach” shown in Figure 6 demonstrates that a port is created in each partition for every power and ground domain that have bumps in that partition. Every port will have a switching current for the chip through that port. The model also contains the on-die parasitic components associated with the P/G network like P/G mesh wire RLC, device diffusion, gate
capacitance, effective series resistance, signal wire RC, well capacitance, intentional decoupling capacitance and resistance, etc. Each port not only captures the parasitics (RLC) present in the partition but also contain the cross-partition coupling information.

Figure 6: Partitioning a design for CPM port

Figure 7 provides a schematic representation of the various elements between a power-ground port pair. The model written in a SPICE format can typically mimic the electrical properties of the P/G network of a chip from DC to 2.5GHz (or more). To validate the goodness of a CPM: (a) run a dynamic analysis of design database along with a package model; (b) capture the switching current and waveform at various port locations, where the ports correspond to the same grouping used in the CPM creation; (c) connect the CPM to the same package netlist and run a SPICE simulation; and (d) compare the switching current and voltage at the ports for dynamic analysis and CPM with SPICE.

Figure 7: Schematic representation of a CPM capturing the switching current and parasitic data

Figure 8 shows the results from a similar exercise as outlined above. As seen from the results, a CPM can capture the overall electrical nature of the on-die P/G mesh network within 5-10% of a rigorous full-chip level transient simulation.
**Experimental Setup and Results**

The experiments to illustrate the relevance of the proposed method used a combination of RedHawk and CPM. The experiment identifies the clock period(s) of interest from a particular input trace pattern or VCD for system PDN analysis, to highlight the worst system-level voltage drop. The flow that was used to perform the experiment is shown in Figure 9. The first step involved simulating the design for the entire duration of a VCD. Then using the FFT based technique outlined earlier, the switching profile from the entire VCD is used to identify the clock periods of interest, containing potentially 1000’s of cycles. Then CPMs are created for these specific clock period(s). These CPMs are then connected individually to the package netlist and simulated using SPICE. CPMs are created for the selected cycles instead for the entire VCD since creating an accurate die model for the entire duration of the VCD is computationally prohibitive and most of the clock periods do not have useful current signature for system PDN analysis.

Figure 9: Proposed flow using RedHawk and CPM technologies.
The library and design database of the ASIC along with the input stimulus file (VCD containing functional mode switching activity at the gate-level) was used to perform a transient analysis for the entire duration of the VCD, which is thirty six (36) micro-seconds long. This step provides the current seen at the chip’s C4 bump locations, coming from the power supply (VRM) through the PCB, package, on-die P/G network, and to the switching cells in the design, while considering various capacitances (and their associated effective series resistance) present in the circuit. However, given the complexity and size of the full-chip level circuit, a transient simulation that is 36us long can take considerable amount of time. Since the goal of this step is to provide the C4 bump level current for subsequent FFT based cycle selection, an advanced accelerated simulation mode employing approximations when extracting the RC network of the on-die P/G mesh, and a higher time-step of 50ps for the transient simulation was used.

The current waveform seen at the chip’s bump locations from this simulation reflects the switching activity and the current demand from the on-die circuit for the duration of the VCD (36micro-seconds) and the filtering effect of the on-die P/G network and other capacitive elements. This composite current profile is then used to screen and identify the clock periods that contain the worst case switching pattern for PDN noise. For this particular design and the VCD used for the experiment, the 36micro-seconds long supply waveform was broken into 4490 sections, each 80 nano-seconds wide and 8ns apart. For example, the first section was from 0 to 80ns while the second section was from 8ns to 88ns. The 8ns shift was chosen to match the PDN resonance frequency of 125MHz and the section width was chosen to cover at least 10 clock periods of 8ns each. Figure 10 illustrates the current profile seen at the power bumps for the duration of the VCD (36us). It also shows in a zoomed in section of the same current profile. The white outline in the zoomed in waveform highlights one 80ns section that was created. The section prior to the one shown will start 8ns earlier while the section subsequent to this one will start 8ns later. Once these 80ns wide sections are identified, FFT was performed to provide the frequency domain representation of the switching current waveform for these 4490 sections of the total current profile.

Figure 10: The total bump level current for the duration of the VCD and a zoom in illustrating the creation of an 80ns wide section.

Figure 11 illustrates the result of the FFT for the first two sections (0 to 80ns and 8ns to 88ns). As evident from this data, the concentration of energy varies from one 80ns
section to another depending on the switching activity pattern. The section width was made at least 10 cycles to make the FFT results more meaningful.

The next step involved sorting these 80ns sections based on the strength of their switching activity around the resonance frequency of the PDN (which for this case was 125MHz). For this purpose, the sum of the amplitude from the FFT for several frequency points around the resonance frequency was calculated for each 80ns section. This parameter is subsequently referred to as fft_sum. It is calculated from the FFT for each 80ns duration as follows: \( \text{fft}_\text{sum} \) (for any 80ns duration) = sum of the amplitude from 110MHz to 130MHz from the FFT data for that duration. Figure 12 shows the value of \( \text{fft}_\text{sum} \) for 4 such 80-ns sections.

These 4490 sections were then sorted based on their respective \( \text{fft}_\text{sum} \) values. From this ranking it was apparent that there was little correlation between the total switching charge (and hence power drawn) and the concentration of switching activity around the resonance frequency. For example, the sections with the highest value of \( \text{fft}_\text{sum} \) did not necessarily have the highest switching power which traditionally is taken as the indicator for highest voltage drop.
Twelve such 80ns sections were chosen from this table (Figure 13). The selection of these 12 sections was done to cover a wide range of switching patterns and coverage around the resonance frequency, by using both the fft_sum and total switching charge as criteria. CPMs were created for each of these twelve 80ns sections at a time-step 10ps for accurate modeling. The CPM for each 80ns section captures the die activity during the specific interval. Ports were created by grouping the C4 bumps into 4 partitions. Each CPM creation step takes about 7 hours on a 64-bit 16GB machine for both transient simulation (80ns duration at 10ps time-step) for the current profile creation and the AC analysis for the die parasitic model generation. These 12 CPMs are tagged as CPM#1.1, 1.2, 1.3, 1.4, 2.1, 2.2, 2.3, 2.4, 3.1, 3.2, 3.3 and 3.4, respectively. They were then individually connected to an S-parameter model of the package and board and simulated using HSPICE. The voltage waveform was measured at the C4 bump locations and compared for these 12 runs.

<table>
<thead>
<tr>
<th>CPM #</th>
<th>Cycle Start Time</th>
<th>End Time</th>
<th>FFT Sum</th>
<th>Avg Cur</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPM3.3</td>
<td>89000</td>
<td>169000</td>
<td>1.782135</td>
<td>0.61</td>
</tr>
<tr>
<td>CPM3.4</td>
<td>137000</td>
<td>217000</td>
<td>1.473784</td>
<td>1.302</td>
</tr>
<tr>
<td>CPM1.3</td>
<td>35648000</td>
<td>35728000</td>
<td>1.2549734</td>
<td>2.91</td>
</tr>
<tr>
<td>CPM1.4</td>
<td>34808000</td>
<td>34888000</td>
<td>1.247208</td>
<td>2.93</td>
</tr>
<tr>
<td>CPM2.1</td>
<td>22056000</td>
<td>22136000</td>
<td>0.8116995</td>
<td>2.28</td>
</tr>
<tr>
<td>CPM2.2</td>
<td>24648000</td>
<td>24728000</td>
<td>0.723724</td>
<td>2.28</td>
</tr>
<tr>
<td>CPM2.4</td>
<td>16969000</td>
<td>1676000</td>
<td>0.67917218</td>
<td>2.29</td>
</tr>
<tr>
<td>CPM1.1</td>
<td>30792000</td>
<td>30872000</td>
<td>0.59617304</td>
<td>2.284</td>
</tr>
</tbody>
</table>

Figure 13: Calculation of energy around the resonance frequency for each 80ns run.

Figure 14 shows the worst peak to peak differential (VDD-VSS) voltage value obtained from these twelve CPM based package/board power delivery simulations. The 80ns durations with the highest value of fft_sum tend to have much higher drops. If two durations have similar fft_sum values, then the average power in the duration determines which one will have higher drop.

<table>
<thead>
<tr>
<th>CPM #</th>
<th>FFT Sum</th>
<th>Avg Cur</th>
<th>Drop (p2p)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPM3.3</td>
<td>1.782135</td>
<td>0.61</td>
<td>345</td>
</tr>
<tr>
<td>CPM3.4</td>
<td>1.473784</td>
<td>1.302</td>
<td>358</td>
</tr>
<tr>
<td>CPM1.3</td>
<td>1.2549734</td>
<td>2.91</td>
<td>141</td>
</tr>
<tr>
<td>CPM1.4</td>
<td>1.247208</td>
<td>2.93</td>
<td>143</td>
</tr>
<tr>
<td>CPM2.1</td>
<td>0.8116995</td>
<td>2.28</td>
<td>107</td>
</tr>
</tbody>
</table>

Figure 14: Table showing, for a group of CPMs created - the fft_sum, average current and peak to peak differential voltage drop (mV).

Figure 15 compares the FFT, current waveform, and voltage waveform from four of the CPMs created. CPM#3.1 is based on one 80ns duration with small current peaks. CPM#1.4, CPM#3.3, and CPM#3.4 are all based on 80ns durations whose current profiles have much higher (compared to CPM#3.1) but quite similar peak current values (around 24A). However CPM#1.4 has similar switching activity in all the ten cycles that
make up the 80ns duration. CPM#3.3 and CPM#3.4 have sparser switching in their 80ns durations with CPM #3.3 having the least switching. However, comparing the voltage drop swing, it is apparent that CPM#3.3 and CPM#3.4 have the worst swings. CPM#1.4 has smaller voltage swing at the C4 bumps even though its associated current profile’s peak values are similar to those seen in the profiles in CPM#3.3 and CPM#3.4 and even though it has much higher power. Note that the noise prediction based on worst case power is 143mV differential peak-to-peak, while the noise prediction based on the FFT criteria is 358mV.

Thus it is evident that if one had chosen the duration of the VCD based on power consumption alone, then the voltage drop seen during the PDN analysis would not be the worst case at the system-level. For die-level analysis, simulating for switching scenarios with higher activity (and hence more switching power) is necessary to identify design weakness, to obtain an optimal power grid network, and to quantify the impact of the drop on the timing and functionality of the design. However for system (package/PCB) PDN design and analysis, on-die switching current with frequency content matching the system resonance frequency creates a higher voltage drop scenario. These types of events

![Figure 15: FFT, current and voltage waveform (at the C4 bumps) for 4 CPMs created using this methodology.](image-url)
typically occur during system power up or when periods of high activity kick-in after a period of low activity. The technique outlined identifies such sequences from an input pattern which can be used for system PDN design and analysis.

**The general methodology**

The methodology to capture the worst case switching pattern has been demonstrated through the above experiment. Although the approach has been demonstrated with a certain tool, it would still be beneficial to deploy this methodology using other tools as well. The major application is to identify the worst pattern among all possible switching cases. Here are the steps for deploying the methodology:

1. Compute the resonant frequencies of the PDN.
2. Generate the current profiles for several switching cases. This can be generated with behavior models or by some types of fast converged approaches with simplified models. The main purpose is to generate as many cases of patterns as possible to represent all the potential switching activities.
3. Perform FFT for all the current profile.
4. Identify the magnitudes of the FFT results of which the frequencies match with the PDN resonance. Choose worst case switching pattern as the case with major components at the resonant frequencies. Perform accurate computation to refine the current profile for the worst case switching pattern.
5. Use this worst case switching pattern for noise analysis.

Note that the accuracy of the worst case prediction strongly depends on the complete collection of all the potential activities captured in the step 2. Thus, it is critical to use tools and approaches which can converge fast to process around thousands of switching cycles with reasonable accuracy.

**Summary**

In summary, it has been highlighted that the interaction between the resonant frequency of the PDN and a major component of the switching current is critical in predicting the worst case noise. When designing the PDN, it is a good practice to analyze the resonant frequency and to avoid the silicon switching frequency accidentally matching with the resonant frequency or its harmonics. A methodology has been demonstrated to capture the worst case switching pattern for noise analysis. By using FFT based cycle selection technology and Chip Power Model, one can create accurate electrical models of the die that allow for accurate time and frequency domain power integrity simulations in the package and PCB level. Ideally one would like to simulate the entire switching pattern available in a VCD. However creating a die model in the form of a CPM for the entire duration of a switching pattern sequence (VCD) especially for large ASIC designs can be computationally prohibitive. Thus, it is proposed to use the technique of identifying durations of interest from a VCD, based on the frequency content of the switching pattern and creating accurate CPM for these specific durations. These CPM views can then be used in SPICE simulations to stress the package/PCB PDN and help guide the placement of appropriate package and system-level decoupling capacitances, help make determination of the amount of decoupling capacitances needed, or help in optimizing the package and PCB layout to reduce the overall noise.