DesignCon 2010

Block level analysis of chip and system level resonances

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Abstract

Power integrity includes the study of impedance profile of power delivery network (PDN) and calculation of voltage noise. This paper demonstrates a block level analysis method to predict and control the resonant frequencies of the on-chip interconnects with the package and board by taking a 45nm chip design as a test case. This methodology helps designers find the locations across the chip where exhibit high PDN impedance and make design decisions in pad placements, decoupling strategy and package selection. It also aids in designing appropriate on-die current waveform for different blocks to analyze the worst-case voltage drop.

Author(s) Biography

Xiaoming Chen: Xiaoming earned his PhD degree from the University of Electronic Science and Technology, China. Now he is working with Qualcomm, Inc. to develop wireless packaging technology. Since 1999 when he joined Nortel Networks Inc., Canada, he has been involving in the design and development of packages and modules for 10/40Gbps and millimeter wave applications. He used to work with Nanjing Electronic Devices Institute, China, where he designed a variety of GaAs MMICs and internally-matched power MESFETs.

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Sorin Dobre: Sorin has received a MSEE from Politehnica University Bucharest Romania. He’s current focus is in low power design, power delivery network analysis and optimization and digital ESL to GDS design methodology development. Sorin has joined Qualcomm in 1999 and his main responsibilities during the last 10 years were in area of low power digital design, design for manufacturing, power integrity, EDA methodology implementation and IP development.

Prakash Vennam: Prakash is a senior R&D manager at Apache design solutions leading the full-wave field solver team. Prior to this, he was a R&D manager at Sigrity Inc, Santa Clara handling PI/SI products, and was a visiting assistant professor at Pennsylvania State University. He has over 60 publications in the areas of electromagnetics and full-wave solvers, and a senior member of IEEE.

Matt Elmore: Matt is the area technical lead at Apache design solutions covering southern California. He handles full-chip cell based power integrity simulations and package analysis.
**Introduction**

The reliability of Power Distribution Network (PDN) is becoming significantly important in the modern low power Integrated Circuit (IC) designs. Extensive studies [1,2] have been undertaken to minimize the impedance level of the PDN, especially to reduce the impedance peak at the resonant frequencies. The PDN resonance is a function of the electrical parasitics of all the interconnect structures between IC, package and printed circuit board (PCB). Consequently, a full system simulation with detailed modeling of each system component as shown in Fig.1 is required to determine and mitigate system resonances.

![Fig.1 Schematic model of global PDN parasitic connectivity](image)

On-die parasitics (Cdie and Rdie in Fig.1) vary spatially over the die. Depending on device density, decap placement, signal and power coupling capacitance, different regions across the die exhibit a non-uniformity of parasitic contribution. If we divide the chip into N x M partitions as shown in Fig.2, the variation of Cdie and Rdie can be observed by examining the impedance looking into any arbitrary port. When the package is partitioned in the same pattern as the die and merged with a PCB, the impedance profile of each cell can be calculated.

![Fig.2 Flip-chip partitioning into domains](image)

We performed a chip-package-board co-simulation by partitioning the die bumps into 3 x 6 regions. The package has six metal layers and the PCB has 14 metal layers. The test chip is developed utilizing TSMC 45nm technology, targeting for mobile cellular phone applications. It has more than 250 million transistors operating at very low voltage of 1 volt. The impedance profiles of the 18 regions are calculated using a 3D full wave electromagnetic (EM) solver. The results reveal that all regions resonate at the same frequency and some regions have even a second resonance. The resonance phenomenon
has been explained with the help of coupled RLC resonators. Numerical experiments have been carried out in line with this theory, which substantiate our findings as to why each region shares the resonance at the same frequency point. The effectiveness of increasing the on-die decoupling capacitance in selectively controlling the impedance in certain cells is presented.

**The 3D full-wave simulation of package and PCB**

Both the package and PCB layout were imported into a 3D full-wave EM tool and merged together. Modeling the package and PCB together captures the higher order coupling effects between them. The die component of the package is then divided into 3 x 6 cells and 18-ports have been setup. The top-view of the package together with port location is presented in Fig.2. The electrical analysis of the entire system has been carried and an 18-port S-parameter model has been extracted. It was assumed that in each region, the on-die parasitic capacitance $C_{\text{die}}$ is 1nF and resistance $R_{\text{die}}$ 10mΩ. Note that at this stage, the mutual coupling between different cells of the chip model is ignored, but the cells are still coupled through the package and PCB. Port-1 is terminated with the series $C_{\text{die}}$ and $R_{\text{die}}$ and port-2 to 18 are left open. The resulting input impedance is presented in Fig.3 (the curve in red.) The impedance peak at 200MHz indicates region-1 has resonance at that frequency. This process is repeated for all other 17 ports. Input impedance of port 7, 13, 14, 15 and 18 are also displayed in Fig.3, which shows a disparity between resonant frequencies. For example, port-15 resonates at 300MHz.

![Fig.2 6x3 chip partitioning into regions. The region numbering is defined as port number in red.](image-url)
Fig. 3 Input impedance at ports 1, 13, 18, 14, 15, and 7. The RC parasitic on-die is assumed to be \( C_{\text{die}} = 2 \text{nF} \) and \( R_{\text{die}} = 10 \text{m\Omega} \) for each port.

In a second simulation, a series \( C_{\text{die}} \) and \( R_{\text{die}} \) is connected to port-1 and 15 at the same time. The impedance curves are depicted in Fig. 4. It can be seen the two ports now resonate at the same frequencies; first resonance at 150MHz with larger impedance amplitude; the second resonance is at higher frequency of 490MHz and has lower impedance amplitude. This kind of convergence in resonant frequency was observed for other ports as well.

Fig. 4 Impedance when \( C_{\text{die}} \) and \( R_{\text{die}} \) are added between ports 1 and 15. The two ports have a resonant frequency at the same location (the curve in dark blue is for port 1 and pink curve for port 15.)
The third experiment involves incrementally adding the series $C_{\text{die}}$ and $R_{\text{die}}$ between port 14, 18, 13 and 17. The impedance at port-1 is simulated for each of the cases and is displayed in Fig.5. The resonance at port-1 is seen to be shifting gradually to a lower frequency when more ports are terminated with a series $C_{\text{die}}$ and $R_{\text{die}}$ circuit. Interestingly, as each RC circuit is added, the resonant frequencies of ports 1 and 15 converge at 90MHz. Again, another resonance peak can be seen at the higher frequency point.

![Fig.5 Impedances when port 1, 15, 14, 18, 13 and 17 are incrementally connected with $C_{\text{die}}$ and $R_{\text{die}}$. Dark blue curve is impedance at port 15. The rest are for port 1.](image)

**RCL resonant circuit simulation**

To study and explore the observation of frequency convergence as shown in Fig.4 and 5, analysis and simulations of the magnetically coupled RCL resonators were performed. Two identical resonators will exhibit a behavior called moding split when there is certain amount of mutual coupling between the resonators [3]. As a result, there are two resonant frequencies in the coupled circuit. One resonant frequency is lower but the other is higher than the natural resonant frequency of single resonator. The RCL resonator circuit we analyzed is shown in Fig.6. The two RCL resonator circuits with different component values result in different natural resonant frequencies. Only inductive coupling effect is considered here without loss of generality.
Fig. 6 Magnetically coupled RCL resonator circuit.

Applying Kirchhoff’s voltage law to the each resonator gives:

\[ R_1 = \frac{E_{12}}{I_1} + \frac{E_{13}}{I_2} \]
\[ 0 = \frac{E_{12}}{I_1} + \frac{E_{13}}{I_2} \]  \hspace{1cm} (1)

where,

\[ E_{12} = R_1 + j\omega L_1 - 1/(\omega C_1), \quad E_{13} = R_1 + j\omega L_1 - 1/(\omega C_1) \]

and

\[ E_{14} = \frac{E_{13}}{I_1} + \frac{E_{12}}{I_2} \]

Then, the input impedance \( Z_{in} = \frac{V_1}{I_1} \) can be calculated from equation (1). By making the imaginary part of \( Z_{in} \) equal zero, we can find two resonant frequencies:

\[ \omega_1^2 = \frac{1 + \omega_2^2 - \omega_2^2 (1 - \kappa^2)}{2(1 - \kappa^2)} \omega_2^2 \]  \hspace{1cm} (2)

where \( \omega_1^2 = 1/\sqrt{L_2 C_2}, \omega_2^2 = 1/\sqrt{L_1 C_1}, \kappa = M/\sqrt{L_1 L_2} \) and \( \omega = (\omega_1/\omega_2)^2 \).

The input impedance equation (1) was verified through a circuit simulation. The circuit schematic of two RLC resonators is shown in Fig. 7.

Fig. 7 Schematic of two RCL resonator circuit.
When no coupling exists, i.e. inductive coupling coefficient $k$ is zero, between the resonators, the impedance plot is given in Fig. 8, which clearly shows two natural resonant frequencies as expected.

Fig. 8 Impedance of the two RLC resonators without coupling.

When the coupling coefficient $k$ equals 0.6, the impedance profile is calculated and displayed in Fig. 9. The moding split resonance can be seen; each resonator has the same impedance peak at a lower frequency ($\text{freq}_{\text{lower}}$) and has the other one at a higher frequency ($\text{freq}_{\text{higher}}$). Further simulations proved that the amplitude of the impedance peak at $\text{freq}_{\text{higher}}$ may be much smaller than that of the impedance peak at $\text{freq}_{\text{lower}}$ depending on the amplitude of the coupling.

Fig. 9 Impedance of the two resonators with magnetic coupling.
The circuit of more than two RCL resonators has been analyzed as well to further investigate the frequency convergence mechanism. Fig. 10, 11 and 12 show the circuit of three resonators, the simulated impedance with and without mutual coupling. The results clearly indicate each resonator has a impedance peak at the same resonant frequency.

![Fig.10 Schematic of three RCL resonator circuit.](image1.png)

![Fig.11 Impedance of the three resonators without coupling.](image2.png)

The simulated results discussed above demonstrated that mutual coupling will force different resonators to have and converge to the same resonant frequency. Inside the package and board, there is both inductive and capacitive coupling across different regions. As a result, each region will resonate at the same frequency.
Co-simulation of chip, package and PCB

Additional simulations were performed using a detailed die model in the form of the Chip Power Model (CPM) technology. The CPM that was created had 18 partitions with VDD/VSS ports per partition. The CPM is generated in an ASCII Spice format and includes both inductive and capacitive coupling. The CPM is connected to the S-parameter model of the package and board generated using a 3D full-wave tool as discussed in Section II. The impedance of each port is given in Fig.13. It can be seen that all the regions resonate at the same frequency.
However, some ports have high impedance above the resonant frequency, such as port-3. We increased Cdie at this port and repeated the CPM-package-board co-simulation. The results show that the high frequency impedance has been brought down (Fig.14).

Summary
An IC-aware system verification has been carried out including the global PDN impedance profile control and resonance prediction. IC profiles such as spatial loading across the die, as well as parasitics of non-linear on-chip devices including decoupling capacitors and loading capacitances are rigorously included in this methodology. A die partitioning scheme based on a block division of the IC pads has been employed. An independent dynamic power analysis at the block level has been carried out to predict the worst case profiles. The block based Chip Power Model (CPM) has then been combined with the full-wave based package and PCB models for the impedance profile analysis. From the worst case analysis results, one can identify the potential areas of concern with the PDN, on a global scale. The impact of block level resonances and their propagation into adjacent domains has been presented. The experimental results demonstrate the effectiveness of the proposed method.

The designers often tend to represent the on-chip network with either a single RC model, or go to the extreme of extracting every bump pad. For a typical flip-chip design, having every bump location extracted is cumbersome and complex for subsequent simulations, if not impossible. However, if one lumps all the bumps together the subsequent model will not capture the distributed nature of the on-chip switching activity and parasitics. The block level partitioning adopted here alleviates the above issue by maintaining sufficient resolution to assess the worst case drop at key areas of the chip. It

![Fig.11 Impedance response from CPM-package-board co-simulation when Cdie at port 3 is increased.](image)
not only captures the parasitics in each block, but also contains the cross-block coupling information. It has been shown in this study that this cross-block coupling is a key factor in controlling resonances at a global level across the chip.

The mathematical formulation presented here support the evidence that these different blocks act as coupled resonators. The complete power impedance seen by the silicon usually resonates at around a few hundred Mega-Hertz (MHz). The on-chip parasitic coupling in combination with the package and PCB routing causes all of the resonant frequencies of different regions to converge. A moding split behavior was observed in our test case, wherein the resonances of each block tend to converge to each other at the first resonance. The second resonances occur at higher frequencies and peak impedance could be very different for each block. Furthermore, the impedance level and voltage drops at critical block can be controlled by selectively the using capacitive loading while taking advantage of the voltage damping provided by neighboring cells. These numerical experiments provide an insight into addressing the design at different regions of the chip thorough a rigorous and accurate full-wave based co-simulation.

Acknowledgements
Authors gratefully acknowledge the key insights provided by Yiwu Tang and Jean Jin of Qualcomm towards explaining the observed phenomenon in terms of coupled RLC resonators.

References