Optimize Power Consumption & Delivery from RTL to GDS

SemiCon Europa 2014
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Apache Design, A subsidiary of ANSYS
It is all about Power!

Power control is mandatory!
How do we control the Power?

Power Control Efficiency is a must!
Use case: Gated Clock

Inefficient controls waste power

Block level enables control significant power

Synthesis will optimize cell level clock gates, but Block level clock gates are even more critical!
Use case: Data Path

Exclusive Cone of Logic driving Mux Input

Redundant Activity wastes Power

Final Gate Netlist Power Performances rely on RTL Code Efficiency
PowerArtist: RTL Power Metrics

Power Metrics

- Peak, Averaged and over time Power
- per Hierarchy, Type, Domain
- X-Probing RTL <-> Schematic
- Any user metrics from API

Efficiency Metrics

- Clock Gated Efficiency
- # non-enabled Registers
- Redundant Memory/Mux Activity
- Data Activity vs. Clock Activity
- Power saving estimates
module PA (
    .
    always @ (posedge clk) begin
        dout <= din1;
    end
)

VHDL, Verilog, System Verilog

User or Automatic
RTL edits

PACE: RTL Power Predictability

Gate Level Power Numbers highly depend on Clock Tree Structures & Signal Routing

PACE bridges RTL vs. Layout gap

Predictable RTL Power Accuracy

Clock tree models, buffers, trees, gating topology
Wire cap models

Layout Gate-level
Activity Analysis coverage

Standard signal waveforms
Judging activity is difficult!

PowerArtist Activity Viewer
Easy to identify unexpected activity

Millions of Cycles can be Analyzed at RTL Level

Frame: CYCLE_POWER
- Start time: 0.0806005
- Finish time: 0.0806007
- Average leakage for supply VDD: 0.002569
- Average power for supply VDD: 0.250168
- Peak power for supply VDD: 0.266678

Frame: DIDT
- Start time: 0.0817704
- Finish time: 0.0817706
- Average leakage for supply VDD: 0.00257393
- Average power for supply VDD: 0.185336
- Peak power for supply VDD: 0.219776

Worst Power
Worst di/dt
module PA {
    ... always @(posedge clk) begin
        dout <= din1;
        end
    assign out = sel ? dout : din2;
    ... endmodule

RTL-to-GDS Power Integrity

PowerArtist

RPM: RTL Power Model
Avg Power, Power over time, Critical RTL vectors

RedHawk

Chip Power Integrity Coverage
Early Voltage & Reliability Analysis, Switching Activity
Early Chip Power Modeling

SI-Wave

Chip-Package-System Integrity
Thermal, Power, Reliability, EMI Analysis
Power Gates’ Efficiency

Integrity concerns with Power Gated Designs
- How long to reach nominal supply?
- How big is the rush current?
- Is the Ramp-Up homogeneous?
- What about the coupling noise with top level?
- What is real “OFF State” leakage?

Power Gates Physical Implementation

Low Power Analysis Results
- Peak-Battery Current
- Peak-Ramp-up Current
- Worst-Ramp-up Current
- Max Differential Voltage
- Noise Coupling
- Worst Switch Current
- Switch 0/1 Sat Check
- Switch 0/1 Off State Check

RedHawk-Explorer
Low Power Analysis Checks

Coupling Noise at Top Level
Instance Voltage over time
Power-Thermal Efficiency

Leakage Dependency on Temperature
Sub-threshold voltage is temperature dependent

Self Heating

POWER
TEMPERATURE
Leakage

Chip-Package Power-Thermal Convergence Analysis

Leakage Dependency on Temperature

SoC Heat Flux, per layer

Package Layout

Thermal convergence
T startPos

Thermal run-away
T startPos

RedHawk™
Chip/Silicon

Sentinel™-TI
Package

Icepak
System

TOP Layer
Metal4
Metal3
Devices level
Substrate

T Maps at # Layers
Converged Power/T
Conducted Heat
Thermal Boundary Conditions
Heat Dissipation
Flagship Technology

ANSYS Fluent™
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- Engine Combustion
- Thermal Management

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- Wireless Connectivity
- Electric Motors, Battery

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- Static Structural
- Vibration and Stress
- Component Design

ANSYS RedHawk™
- RTL2GDS Power Noise
- Foundry Certified Reliability
- C-P-S Power, Signal, Thermal
Thank you

Merci