Power and Thermal Simulation Considerations for Stacked Die Packages

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Outline

- Stacked die design multi-physics challenges
- Power and noise modeling
  - Concurrent and model based approaches
- Thermal modeling
  - Impact on power, reliability and timing
- Ongoing work
Stacked Die Design Needs

- Multi-physics challenges:
  - Electrical-, thermal-, and mechanical-aware design
- Cross-domain, organization, company

Simulation Goals

- Exploration and planning
- Analysis, optimization and sign-off
Simulation Needs for Stacked Die Designs

- **Voltage Drop and Power Noise Impact**
  - Top die experience additional voltage drop and coupled noise from lower die or interposer in the stack-up
  - Presence of TSV farm and associated metal/via affect the homogeneity of power delivery network (PDN) for the bottom die

- **Thermal Impact**
  - Thermal profile due to combined power and thermal signature from shared micro-bump connections
  - Significant impact to power (leakage), reliability (EM) and timing (hold)
Simulation Approaches for Stacked Die Designs

- **Power**
  - Model based
    - Compact, IP protection
    - Simplified and open format

- **Thermal**
  - Concurrent
    - Simultaneous analysis
    - Multiple layout/result display

- **ESD**

- **Signal**
Model Requirements for Stacked Die Analysis

- Contain self-consistent electrical data
- Enable seamless connections to other models or to chip/interposer layout
- Be in open standard format
- Simplified topology to enable analysis
  - Power estimation
  - Power noise: DC and time-domain
  - Impedance analysis (frequency/DC)
  - Reliability analysis (EM, ESD)
- Similar or integrated model for thermal
- Contain technology / design parameters
Model Based Stacked Die Analysis
Self-Consistency of Model

Full layout based analysis

Model based analysis

Model Based Stacked Die Analysis

Open Interface Protocols

- Streamlined import and hookup
- Define model creation options (static, dynamic – VCD/V-less)
- Define content for stacked die power analysis (estimation, drop, …)

Detailed Chip Layout

CIP Header

```
* die_area 0 0 6000 4000
* VCC_1: (250 250) : p1 = PAR_0_0_VCC
* VCC_2: (500 250) : p1 = PAR_0_0_VCC
* VCC_3: (750 250) : p1 = PAR_0_0_VCC
...
* VCC_1: (100 100) : p2 = PAR_1_0_VCC
```
Case Studies of Stacked Die Design Analysis

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Concurrent analysis: Voltage drop on both die

Comparing concurrent versus model based

Case Studies of Stacked Die Design Analysis

3D Design description:
- Logic/logic face-to-face stack
- 32 nm top die
- 65 nm bottom die
- Package

TSV placement optimization

Top Die IR map with bottom die included

Bottom die IR map with top die included

Model Based Thermal Analysis

CTM: Chip-Thermal-Model, Temperature dependent library of power maps for each chip

3D Temp Profile layer-by-layer

IC Designers
Power, EM Analysis

System Designers
Cooling System Design

Thermal Model
θ-JA/JB/JC, Delphi
Case Study: Model Based Thermal Analysis

Thermal hot spot in the bottom die on the lower right corner (aligned with power density hot-spot)

Thermal hot spot in the top die on the lower right corner (due to heat sharing from uBumps)
Stacked die analysis presents several multi-physics problems.

Good models are necessary to bridge design and organization silos.

Apache is working on several areas:
- Stacked die power noise simulation
- Stacked die thermal and mechanical stress modeling
- Reliability and timing analysis

Working with Si2 on Open3D initiative.