Chip-Package Co-design Time and Frequency Domain Analysis

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Problem Statement

- First generation design failed to meet timing requirement
- Second rev of design passes with increased on-die capacitance
- Both revs of the design had similar static voltage drop

Transient simulation with package indicated otherwise

- Rev 1 had significantly higher droop

WHY?
Why Would Static Miss a Failure?

Fails to Consider:
Chip-Package-PCB Coupling / Resonance
Simultaneously Switching Instances
On-die RLC and transient current
What Do We Need in a Dynamic Simulation?

\[ V_{dd} \text{ Pad} \rightarrow i(t, V) \]

Switching instance

\[ V(t) \]

Switching instance

\[ i_s(t) \]

Non-switching instance

\[ i(t, V) \]

Non-switching instance

\[ C_{pg} \]

\[ C_{load} \]

\[ C_{dev} \]

\[ R_{load} \]

\[ ESR \]

\[ C_{dev} \]

\[ C_{load} \]
Modeling the Impact of Package / PCB

Chip DvD can be exacerbated from:

(a) High L from Package / PCB
(b) High Di/Dt from on-chip switching
(c) Resonance between package/PCB and chip

Resonance frequency

Test Case Details

Rev1 shows significantly higher dynamic voltage drop.

Both revs show similar (low) static voltage drop.

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Time Domain Analysis Using RedHawk™

Red – Chip activity

Yellow – Supply current (no pkg)

White – Supply current (rev1, with pkg)

Blue – Supply current (rev2, with pkg)

Red – Voltage at Pads (rev 2, with pkg)

Yellow – Voltage at Pads (rev1, with pkg)
Frequency Domain Profiling of Switching Current

Time domain waveform

current2fft ....

FFT of chip activity current indicates peak energy @ 74MHz
Chip-Package-System (CPS) Frequency Domain Analysis Using CPM

- Chip on-die Power Grid RLC
- Transistor current /cap/ESR
- Open SPICE netlist format

Chip Power Model (CPM™)

CHIP + Package

C4 bumps

CHIP

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Frequency Domain Analysis of CPM+PKG

- Rev1 (yellow) resonance freq ~ 68MHz
- Rev2 (red) resonance freq ~ 43MHz

- Rev1 “resonance frequency” around chip activity of 75MHz

Why Does Resonance Frequency Shift?

AC analysis of package alone:
L_eff of package = 149pH

Resonance happens at: \( \omega L = 1/(\omega C) \).

- \( C_{REV2} = 1/((2*\pi*f_{resonance})^2*L) = 1/((2*3.1415*37.39e6)^2*149e-12) \approx 121nF \)
- \( C_{REV1} = 1/((2*\pi*f_{resonance})^2*L) = 1/((2*3.1415*59e6)^2*149e-12) \approx 49nF \)
Summary

- A traditional DC/Static voltage drop approach does not model capacitive and inductive elements in a chip-package PDN.
- Time and Frequency domain analysis are needed to accurately predict Ldi/dt and resonance impact on the chip package system.
- In this example, we found that the additional on-die capacitance in Rev 2 shifted the chip-package resonance frequency, significantly reducing the voltage drop.