ESD Dynamic Methodology for Diagnosis and Predictive Simulation of HBM/CDM Events

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50 Words Abstract – A comprehensive ESD dynamic methodology is developed for failure diagnosis and predictive simulation of improvements. This methodology focuses on dynamic analysis including modeling of die-level metal grid, substrate grid and well-diode, package effective capacitance, and pogo pin. Real HBM and CDM application examples are illustrated.

I. Introduction

Although a full-chip geometry-based ESD static check of resistance and current density is available [1], it cannot catch all HBM/CDM issues, particularly when problems are not resistance dominant. So, an ESD dynamic simulation approach is needed to complement the static solution [2]. In particular, a transient transistor-level simulation is needed to detect weak or stressed junctions, and monitor current/voltage on transistor ports and wires. Modeling can include coupled signal RC network, metal grid RLC network, package model, pogo pin RLC model [3,4], substrate RC network and well-diode for metal grid and substrate discharging paths, particularly for CDM events. Some dynamic solutions may not have detailed metal grid RLC and substrate RCD (RC and well-diode) extraction, or else involve manual steps in their approach [5,6,7]. This paper proposes an ESD dynamic methodology for checking block-based HBM/CDM discharging events for diagnosis and predictive simulation. The methodology uses help from PathFinder-D [8], a tool that constructs dynamic ESD circuits with complete parasitic models in simulation.

II. ESD Dynamic Analysis Methodology

This paper outlines an ESD dynamic methodology intended to achieve the following goals:

1. Perform diagnosis of potential failure mechanisms when silicon failures occur.

2. Verify fixed solution robustness by comparing differential stressed values of the failed junctions.

3. Check potential design weaknesses of HBM/CDM events before tape-out of analog/mixed-signal/IO blocks.

To achieve these goals, we build upon the ESD dynamic tool in the flow for block-based diagnosis, fix verification and predictive simulation.

There are two reasons a full-chip ESD dynamic simulation is not performed in our flow. Instead, a block-based dynamic simulation containing up to 1M transistors covering most of the analog blocks is run.

First, most HBM/CDM problems are localized
and can be determined from a smaller block-level simulation. We verified this assumption by testing a small block by itself and also by testing a much larger block containing the smaller block, where the same stressed junctions were found to be flagged in the same correct ranking order, although the absolute stress levels were different. The smaller absolute stress levels seen with the larger block as compared to the smaller block is due to more discharging paths involving more parasitics, larger areas for substrate current distribution, and possible current discharge through remote clamps.

Second, block-level simulations are preferred due to capacity limitations. Block-level simulations can be handled in the flow with reasonable time and memory usage, although capacity improvements are ongoing. The following section describes modeling of the individual components and input/output in the proposed flow.

**III. Modeling for ESD Dynamic Simulation**

To achieve silicon correlation of HBM/CDM diagnosis on stressed junction failures, we considered modeling various parts of the package including the die. Due to the fast transient discharge waveform for CDM events, the model must include the on-die metal grid RLC, pogo pin RLC, package RLC, and high-voltage transistor models. We also needed to model the diode/clamp, silicon substrate, and package substrate-to-ground capacitance, as described below.

**A. Clamp Modeling**

The ESD clamp cell is described using its I-V characteristics (Figure 1). This I-V curve can be obtained from a Transmission Line Pulse (TLP) measurement or from a device-level simulator. The dynamic simulator takes the I-V curve and translates it into a behavior model that is specially tailored for its snapback characteristics by the tool’s simulator. If the ESD clamp does not have snapback characteristics such as an RC-based clamp, the original circuit can be simulated directly without I-V behavior models. However, due to typically lack of high-voltage BSIM transistor modeling, the measured I-V curve of the RC-based clamp often can carry more current than that based on BSIM models. Therefore, a TLP-based I-V curve for the RC-based clamp can also be used, although it does not exhibit snapback characteristics.

![Figure 1: Typical I-V curve for a snapback clamp and I-V curve for a diode is a degenerated case with Vh=vt1.](image)

**B. Signal and Metal Grid Modeling**

The coupling between a signal net to other signal nets and Power/Ground nets is very important for modeling accurate discharging paths. Thus coupled Power/Ground nets extraction for RLC modeling is done in the tool, while coupled signal nets are extracted using typical cell DSPF (Detailed Standard Parasitic Format) extraction flows. On-die inductance extraction is needed due to the fast slew rate (~200psec range) of CDM discharging events, and is most likely not needed for HBM discharging events (where slew rates are in the order of several nanoseconds).

**C. Die Substrate Modeling**

The chip substrate also plays an important role in ESD simulation [9]. The tool extracts substrate parasitics (RC) and well diodes based on physical layout/GDS geometries and substrate tech file information. In the substrate tech file, per substrate layer resistivity and per unit capacitance are given. Additionally, the diode model for pwell-to-nwell junctions is typically available from the foundries (Figure 2).
Figure 2: Substrate modeling for RC extraction and distributed well-diode.

D. Package Substrate-to-Ground Capacitance

For CDM testing, there is a package substrate to ground capacitance between the package and the charging plate (Figure 3) [10,11]. Since distributed capacitance is connected to the bottom of the die substrate, this can directly affect the pogo pin peak current. We employed a methodology that automatically tunes this capacitance so that the peak of the pogo pin current matches the known or estimated peak current from the CDM lab test. This provided the same pogo pin peak current condition in the simulation as in the lab test. Since the block being simulated in only part of the full-chip, the simulated peak current going into the block may see a larger stress due to a lack of the surrounding RLC network outside of the block. However, our focus is on the relative ranking of the highest stressed junctions, and not on the absolute stress value which is more difficult to predict especially when parasitic BJT’s are involved in the discharging paths. Since we are looking for the weakest and most stressed junctions before the effect of any parasitic BJT’s, we typically assume that parasitic BJTs will not turn on. However, if needed, the effect of parasitic BJT’s can be included by incorporating the I-V curve for modeling parasitic BJT’s between D/S nodes of transistors [12].

Figure 3: The capacitance definition for substrate_to_gnd_cap, courtesy J. Karp, EOS/ESD Symposium, 2008[10].

E. Block-based ESD Dynamic Flow

The key steps are summarized. The flow parses the original input DSPF netlist which was generated with coupled signal RC extraction, then generates the device/tap contact points to connect to the P/G/Substrate network (Step 1). It then extracts the parasitic RLC network of Power/Ground grid, substrate RC network, and distributed well-diodes (Step 2). By combining the two netlists, a complete design netlist is obtained. Finally, PathFinder-D creates a test bench (Step 3), based on the zapping pin condition for a given ESD mode (HBM or CDM) and simulation settings, then proceeds on to the ESD dynamic simulation. The overall ESD dynamic flow is shown (Figure 4). Once the simulation is completed, the ESD stress analysis (Step 4) is performed, based on stress thresholds of devices provided by the user.

The ESD dynamic simulator can handle approximately 1 million transistors in transient simulation. After obtaining the simulation results, it can perform stress analysis and report the design’s weak junctions. Users can perform ESD failure/weakness diagnosis within a function-rich GUI, cross-probing between reports and color maps, movie, or waveforms in order to debug and identify design issues related to ESD events.
IV. Application Examples

In this section, both HBM and CDM discharging events are illustrated in application examples using the described ESD simulation methodology.

A. HBM Discharging Event Example

This HBM discharging event case is of an I/O block with 12k mosfets, 6k diodes, and about 6M RLC elements of metal grid RLC, substrate RC, and package netlist, as shown in Figure 5.

The simulation for the HBM -2000V zap set-up on the AGND pin with AVDD pin grounded with 10nanosecond discharging time takes about 16 hours and uses 15GB of system memory. The HBM AGND pin zap analysis predicts failure at -2000V when the RC clamp’s substrate pwell guard-ring is grounded. The failure spot is at the center finger of the RC clamp. However, the similar I/O block AGND pin zap passed when the pwell guard-ring was floated in a modified/fixed version of the I/O (Figures 6 and 7). The substrate grid extraction resolution is 5um while the RC-based clamp is about 300um in width, so each finger’s substrate node can be captured.

Through ESD HBM dynamic simulation, we can see that the Voltage across bulk and source nodes (Vbs) of different fingers of the RC-based clamp varied, with the center finger’s Vbs being the largest in the pwell guard-ring grounded case, while very little Vbs variation is seen in the pwell guard-ring floated case (Figures 8 and 9). A dynamic HBM movie showing all junction voltages versus time can illustrate the exceeded stress in the middle finger of the RC-based clamp, a snapshot of which is shown in Figure 10.

Figure 4: Block-based ESD dynamic flow.

Figure 5: HBM -2000V zap on AGND pin, and with AVDD pin grounded for an I/O.

Figure 6: Comparison of HBM result with/without pwell guard-ring grounded in RC-based clamp.

Figure 7: HBM -2000V zap on AGND pin, and with AVDD pin grounded for an I/O.
Figure 8: Vbulk has more variation; center finger has highest value on pwell guard-ring grounded case. Same Vsource for all fingers, so center finger has largest Vbs.

Figure 9: Vbulk shows little finger variation on pwell guard-ring floated case. Vbs is same for all the fingers since they have the same Vsource.

Figure 10: Dynamic HBM simulation movie shows the junction voltages versus time, with red color indicating exceeded stresses.

The theory of failure is that the clamp fingers’ parasitic bipolar devices turned on unevenly due to the uneven distribution of Vbs voltages. This is because the center finger is farthest from the P+ grounded guard-ring, therefore it has the largest resistance from the AGND zap point. The Vbs of the center finger is also higher because its substrate node is farther away from the P+ grounded guard-ring. Therefore, the center finger has the highest Vbs, and therefore likely to exhibit earlier breakdown that is suggested from the simulation result. An uneven breakdown channels ESD current into a localized region causing point damage as shown in Figure 11, taken from Lab FIB test on a HBM tester manufactured by Thermal Fisher, Model MK4.

Figure 11: Lab FIB test of failed HBM test on I/O with pwell guard-ring grounded.

B. CDM Discharging Event Example

The second example is a CDM failure with a -500V zap on IOP pin, 62K mosfets, 700 diodes, and approximately 3.7M RLC elements of metal grid RLC and substrate RC, as shown in Figure 12. Realistic model values of Lpogo, Rpogo, and Cpogo are used [4, 5]. The simulation takes about 12 hours and uses 25GB of system memory for 1.5nsec of simulation time, 1psec time step.

Figure 12: CDM failure test case with -500V zap on IOP pin.
For CDM testing on a large chip, the CDM pogo pin current waveform is defined using JEDEC CDM testing standard [JEDEC2004], as shown in Figure 13 and 14.

From the CDM test measurement, the peak pogo pin current waveform of the chip with ~100M instances is about 7Amp. With settings of Rpogo (25Ohm), Lpogo (5.5nH), and Cpogo (0.1fF), PathFinger-D automatically tunes Csub (composed of Cpkg_to_gnd and Csubstrate_to_gnd) to match the -7Amp peak pogo pin current set forth by the user.

In this CDM discharging event example, while the global ESD protection scheme takes care of the bulk of the current discharge, the instantaneous charge distribution around the failed junction is highlighted in a circle, as shown in Figure 15, and is beyond the speed of what can be handled by standard protection schemes. The I/O node discharges very rapidly and the gate node of the failed junction forms the center node of a capacitive voltage divider (Cgate in series with Cbiasload). In this circumstance, the gate node cannot discharge as rapidly as the I/O node can. Thus, a potential voltage difference builds up beyond the limit of the gate oxide tolerance range and causes device damage.

Figure 16 references a typically measured waveform on a calibrated tester, showing the CDM event and illustrates the high speed of these events as it starts and finishes with a slew of about 300psec. Figure 17 shows the simulated pogo pin current waveform with the peak current calibrated to -7Amp. The slew/overshoot/undershoot follows the JEDEC guideline, particularly with a worst case slew of about 180psec. Standard ESD devices typically only operate after the damage is done and has no ability to keep the junction voltage low enough to withstand the discharge event. We speculate that only the -500V zap shows this problem due to the bias net being heavily referenced to ground. In the +500V discharge scenario, current flow through diode to ground is fast enough to pull the ground net closer in potential with the I/O pin. In this case, both ends of the series capacitor divider drop together, so there is no voltage build up between the bias net and the I/O pin. Both the positive and negative zap stressed junction waveforms are shown in Figures 18 and 19. These demonstrate that there is less stress in the positive zap case versus high stress in the negative zap case on the same worst stressed junction (from the negative zap). Figure 20 pinpoints the location of junction damage shown in the FIB image. It was performed on a CDM tester manufactured by Thermal Fisher, Model Orion.
Figure 15: Impedance mismatch between I/O (sig) net and LDO output net caused large Vgd junction stress with negative 500V zap on signal pad. LDO is low drop-out on-chip voltage regulator; PC is power clamp between Vdd/Vss nets.

Figure 16: a typically measured pogo pin current waveform on a calibrated tester with about 300psec slew.

Figure 17: Using CDM dynamic simulation, pogo pin current conforms to the JEDEC standard.

Figure 18: Worst stressed junction Vgd waveform based on CDM dynamic simulation on negative zap.

Figure 19: The same stressed junction (from negative zap) Vgd waveform based on the CDM dynamic simulation on a positive zap.

Figure 20: Lab FIB test, failed CDM test on I/O cell for -500V zap on IOP pin.
As a potential fix, we manually added a resistance implemented as a PMOS passgate at the gate of the failed junction, as shown in Figure 21. The addition of a series resistor at the gate of the failed NMOS serves to isolate the junction from the loading of the bias net. This isolation allows the junction voltage delta to stay within device tolerance. Obviously, the larger the resistance value is, the more effective the isolation would be from an ESD point of view. The maximum resistance value is determined by normal functional mode requirements. However, the gate resistor does reduce bias voltage stability during normal circuit operation.

As we expected, the stressed waveform on the junction (Vgd) with the PMOS passgate modification shows that a much smaller stress is observed, as Figure 22 illustrates. Different types of potential fixes can be tried using this methodology; preventing a costly and time-consuming fix cycle from the actual design fix tape-out and CDM silicon measurement alone.

![Figure 21: CDM test case with the PMOS passgate fix inserted on the gate node of the stressed junction.](image1)

![Figure 22: Worst stressed junction Vgd waveform based on CDM dynamic simulation on a negative zap with the PMOS passgate fix.](image2)

**V. Summary**

We have outlined a comprehensive ESD dynamic methodology for diagnosis and predictive simulation of HBM/CDM discharging events. This solution can assist ESD designers with insights into the failure mechanism and can also provide comparative stress results of potential mitigating fixes prior to tape-out. This methodology was used to correctly identify the exact failure points of our HBM/CDM real-life examples and to verify the improved modifications.

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**References**


