A design methodology using Power-Grid Prototyping to optimize Area Performance of SoCs

Abhishek Nigam, STMicroelectronics
Bhanu Prakash, Senior Technical Manager, STMicroelectronics
Anant Narain, Apache Design Solutions (a sub. of ANSYS Inc.)

Noida, India

Abstract:
Set-Top-Box (STB) SoC designs are extremely complex with multi-million standard cells, higher core utilization of around 70-80%, and multiple clock domains including high and low frequencies. An assessment of any overdesign in the power grid of such SoCs becomes one of the key competitive business needs.

This paper first describes a methodology for power grid optimization leveraging early static IR flow and correlating with existing sign-off results. It also presents a methodology for doing early dynamic IR drop analysis, which can identify potential overdesigns in the grid to save valuable signal routing area. It outlines the impact of Metal6 power grid width variations on Static and dynamic IR drop using STB SoC in 40 nm Wire bond chip.

Finally, results and conclusion of changing metal density on static and dynamic IR drop analysis at early stage using ANSYS-Apache’s RedHawk tool are presented. The correlation of early results with final results observed are encouraging for decision-making in shrinking metal6 width to gain advantage in routing tracks and consequently floorplan change which can reduce the die-size - a value-add to SoC designs.

Introduction
Set-Top-Box SoC designs are complex, typically with over 5 million standard-cell instances, having multiple frequencies and low voltage supply of 1.1V in 40 nm technology node. In this paper we describe a methodology using a fast PG mesh prototyping based flow for such SoCs, that can be used to identify PG grid overdesign by early static and Dynamic Voltage Drop analysis of the power grid and hence identify opportunities for freeing up valuable signal and clock routing resources on higher metal layers.
The Figure 1 shows the technology inputs, automation scripts for translation of design inputs to the flow and the what-if analysis with metal change variations in power grid. The Figure 2 below shows the layout of the PG mesh prototype of the SoC.

To estimate the effects of PG mesh optimizations on Dynamic Voltage Drop (DvD) analysis, the entire power grid area is modelled as 10x10 regions as in Figure 3. The currents and decaps for each region were estimated from the first PnR database results and provided as APL (Apache Power Library) currents and cdevs models in Figure 4 for DvD analysis with Ansys-Apache’s RedHawk tool.

The PG Mesh in the SoC consists of M1, M6, M7 and AP layers. We have used this methodology to investigate for possible overdesign in the M6 PG mesh. Since most of memories, macros and IPs use the M6 layer, any optimization in the PG mesh of this layer could free useful signal and clock routing resources for hence potential reduction in the area.

For the prototype model validation we used standard 3.4u width of the M6 layer which is the same as used for the first version of PnR database of this SoC. We then investigate using this fast iterative PG prototyping flow, the effect on static and DvD drops versus routing area savings achieved with M6 widths of 2.5u and 1.7u respectively as in figure 5.

Results, Analysis and Conclusions

Static analysis histogram comparing the effect on IR drop for vdd and gnd for different widths of M6 layer is shown below in Figure 6a and 6b resp.
The static-IR color maps between the PnR database (1st version) and PG prototype base static IR correlate well with pessimism of 4mV as. The Figure 7 shows the color maps for M6 widths reduced to 2.5μ and 1.7μ respectively.

A first PG prototype Early Analysis run was done to have the same PG mesh specs as the sign-off database (M6 width 3.4μ) to validate the QoR of this methodology. The Static IR drop color maps for vdd/gnd match reasonably well (Figure 7) with the PnR database results with a pessimism of 4-5mV on vdd and gnd IR drops. Total Veff drop for PnR database signoff run is 3.4% while for Early Analysis run is 4.2%. The Early Analysis results are within +1% of signoff results. The M6 metal width was reduced by ~25% and ~50% of original M6 width by reducing the width to 2.5μ and 1.7μ resp keeping the pitch same. The Veff static IR drop is increased by 0.6% and 1.4% resp. The effect of decreasing M6 width from 3.4μ to 2.5μ is not much. Even the extreme case of reducing the M6 width to half (1.7μ) results in 1.4% increase in static IR. So from the experiments, reducing the M6 density looks feasible as in Figure 8.

Dynamic Voltage Drop analysis histogram comparing the effect on IR drop for vdd for different widths of M6 layer in Figure 9.

The first version PnR database based demand current (sum of all instantaneous currents over time) is shown in green in Figure 10 and battery current (sum of current supplied by the pads over time) is shown in red. The total demand current and battery currents for the grid prototype based early dynamic run are shown in blue and pink resp. and match well with the PnR database runs.

The DvD hotspots in Figure 11 match well between the 1st PnR database based results and the grid prototype based early DvD results using our methodology. The increase in DvD drops due to shrinking M6 widths is marginal and hence the potential routing area savings by shrinking M6 width looks feasible.
The potential savings in routing area for Metal6 are shown in Figure 12.

Recent Silicon results shown in Figure 13 below correlates with pre-silicon simulation results which increases our confidence in the methodology for a new area efficient product.

**Conclusions**

SoC Power-trends of Static and Dynamic Voltage drop with reduced M6 power mesh density was demonstrated on representative SOC which shows a gain in area savings of 6.2 sq-mm and 11.7 sq-mm for reduced widths of 2.5u and 1.7u widths respectively from the signoff width of 3.4u with marginal increase in static IR and DvD drops.

This approach led to the development of a specific CAD method, which has potential for re-use.

**Acknowledgements**

Rajeev Srivastava, ST Microelectronics, India
Naveen Sharma, STMicroelectronics, India
Sachin Mathur, ST Microelectronics, India
Manish Kumaria, STMicroelectronics, India
Ajay Miyan, STMicroelectronics, India
Steve Docker, STMicroelectronics, UK
Guido Angelo Repetto, STMicroelectronics, France