Simulation and Characterization of GHz On-Chip Power Delivery Network (PDN)

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Abstract
A correlation study for on-die Power Delivery Network (PDN) is performed by comparing measurements and simulations. A novel test vehicle, RF silicon-to-simulation (sil2sim), is designed to determine the on-die PDN performance. It comprises only power and ground domains with power grid and on-die decoupling capacitor (decap). Three types of structures are implemented: power grid with on-die decap, power grid only – open, and power grid only – short. These structures are simulated with the external commercial tool RH_PG. The measurements are done using on-wafer VNA, and correlated with simulations. The detailed models for the power grid and the decoupling capacitor are extracted.

Author’s Biography
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**Introduction**

On-die Power Delivery Network (PDN) plays a very important role in the overall system performance over GHz speed. The major components of the on-die PDN are on-die capacitance (C\text{die}) and power grid. The on-die capacitance has parasitic resistance (R\text{die}). The power grid parasitics include grid resistance (R\text{grid}), grid inductance (L\text{grid}), grid capacitance (C\text{grid}) and grid conductance (G\text{grid}). Accurate modeling of on-die PDN elements is essential in the system design. These parasitics are frequency dependent, so they may influence PDN differently at different frequencies. At higher frequencies, inductive and conductive effects become significant.

In the past, various ways have been suggested to generate a power grid model using R, L, C parasitics [1-4]. In this paper, we demonstrate a simulation approach with an external commercial tool RH\_PG. This tool can take the grid layout file and extracts the the RC parasitics. Then, it can reduce the grid netlist to the limited ports specified by the user. It is essential to validate the performance of the grid modeling techniques with the actual silicon structures.

In order to validate the on-die response, a RF silicon-to-simulation (sil2sim) vehicle has been designed. PDN self impedance (Z_{11}) measurements for the silicon are performed using Vector Network Analyzer (VNA). From the measurements, the characteristics of the power grid are extracted and compared with the simulations. Also, the frequency dependent model for the C\text{die} is extracted.

**Test Vehicle**

The test vehicle consists of several silicon e-test pad-row structures on which parametric RF measurements can be performed. These e-test pad-rows are chosen to simplify the measurements using automated RF parametric testing equipment, and for ease of layout execution and repeatability. The following sections explain in detail the e-test pad-rows and the various on-die PDN experiments.

**E-test Pad rows**

The basic layout of an e-test pad-row is shown in Figure 1. In general, the pad-row consists of two rows of metal pad structures. The metal pad structures are at least 50umx50um in dimension, and the distances between the centers of adjacent pairs of metal-pads are between 75um and 100um. A distance of at least 75um is ensured between the centers of adjacent metal-pads to minimize the effects of noise and ISI during RF signal measurements.

The pad-rows are developed on Intel technology that has at least five layers of metal interconnects. The signal (VCC) pad-rows and ground (GND) pad-rows are constructed differently. Each VCC pad is surrounded by GND pad on both sides. The top-most VCC metal layer is isolated from the remaining metal layers by removing the via structures from metal 2 to metal 5. Also individual VCC pad is isolated from the neighboring VCC pad on the same row. For example, in Figure 1, the VCC pad no. 2 and pad no. 4 are not
Figure 1 Schematic of pad-row layout for RF testing

connected together for the VCC domain. Via structure is placed between metal1 and metal2.

The GND metal-pads are so built that all five metal layers are shorted to each other using an extensive network of via structures between each metal layer. Also, all the GND pads are connected together. In between GND and VCC pads, ground shield is provided. This VCC and GND configuration increases the efficiency of RF measurements and minimizes noise and extraneous effects during RF testing. Figure 2 shows a pad-row without the DUT.

**Construction of PDN DUTs**

On a global level, the DUT consists of the PDN, which internally is a combination of a power-metal-grid network and a device-capacitance. Several flavors of device-capacitors are built using different transistor types (native devices, thick-gate devices, etc.). The gate

Figure 2: Sil2Sim pad-row without the DUT
of these devices is routed to the signal (VCC) pads, and the shorted drain-source-bulk terminals are hooked to the GND pads. The metal power-grid-network is an integral part of the PDN and acts in series to the device-capacitors. A pad-row with the DUT is shown in Figure3. The power grid is only connected to the pad-row structure on metal2 and metal7. For in between metals (metal3 to metal5), the power grid is isolated from the pad-row structures.

For RF testing, different pad-rows are built to provide open and short calibration capabilities to the RF (VNA) testers. The open and short structures are built, to allow for characterization of the power grid and the device-caps individually, and also as a single functional-unit. There are three types of structures used for the measurements:
1] Pad-row with the open circuit power grid and capacitor.
2] Pad-row with the open circuit power grid (no capacitor)
3] Pad-row with the short circuit power grid (no capacitor)

Silicon Testing
The pad-row testing is conducted using a cascade semi-automatic wafer probe station. The silicon wafers are directly loaded to these testers, and micro-manipulators are used to position probes for RF testing on each DUT. The probes themselves are custom-ordered to match pad-row dimensions, and have probe-tips comprised of a Ground-Signal-Ground connection internally, as shown in Figure 4. An Agilent Vector Network Analyzer (VNA) E8358A is used to perform the RF measurements, as shown in Figure 5. The probe-tips are first calibrated using a standard-substrate to calibrate parasitic all the way to the probe-tip.

Simulations
Commercial tool RH_PG is used for the power grid modeling. First, RH_PG takes the design layout (GDS) and converts it into DEF/LEF standard design description then extracts the detailed R or RC for the power grid. The extracted netlist is usually very large. The next step is to identify ports on the proper metal layers where the connection to the circuit and power/round is required. The Grid RC reduction takes the extracted
Figure 4: Probe-card measurements on a wafer using two GSG probe-tips.

Figure 5: RF Measurement setup using an Agilent VNA
network of resistors and capacitors that represents the power / ground grid and generates a much smaller electrical network whose frequency domain response at the specified ports for the specified frequency range matches that of the original network with tolerances better than 0.2 %. The resulted network that consists of R and C elements is exported as a SPICE netlist. The reduced netlist is guaranteed to be passive by construction, thus suitable to be used in transient simulations with SPICE or another transient simulator. This netlist can be used with any version of SPICE (such as HSPICE from Synopsys or Eldo from Mentor Graphics, etc.) as it only uses classic circuit elements.

The RC grid reduction starts by calculating the exact short-circuit admittance (Y) matrix of the RC network at ports in the specified frequency range. The frequency range can be set by the user, with the default being from 0 (DC) to 2.5 GHz with the uniform step of 0.1 GHz. This Y matrix is written to a “Y-matrix” text file. The non-strict lower triangle of the matrix is written in real-imaginary format, meaning that Yij for i ≥ j are displayed for each frequency value.

Example for N=3 (3 port)

Freq Y(1,1) Y(2,1) Y(2,2) Y(3,1) Y(3,2) Y(3,3)

After the Y matrix is calculated, the code performs a constrained rational approximation to be exact at DC. This rational approximation with real poles allows the synthesis of R, C (sometimes also L, and G) topology that represents this network at ports. The number of ports should not exceed few hundreds (200). The number of devices in the “reduced” network scales as a square of the number of ports. Thus it’s best to constrain the number of ports as few as needed.

The code generates the SPICE subcircuit for the reduced network. If capacitors to global ground are present, it will have N+1 terminals (where N is the number of ports). The last terminal will typically be connected to the global ground (SPICE node 0) when used. If no capacitors to global ground are present, the code generates a subcircuit with N terminals. The accuracy of the RC reduction approximation is captured in a “fitting” file.

This file shows fit quality for the so-called G matrix defined as

\[ G_{ii} = \sum_{k=1}^{N} Y_{ik}(1) \], and

\[ G_{ij} = -Y_{ij}(i \neq j) \] (2)

The physical significance of G matrix thus defined is that the frequency-dependent admittance Gkk is connected from port k to ground, and Gkl is connected between ports k and l.
Measurements and Post-processing

Measurements are done on all three types of structures, with the VNA: 1] Power grid and decoupling capacitor (decap), 2] Power grid - open, and 3] Power grid – short. S parameters are obtained with the measurements. The terminology used in this paper for these three S parameters are Stotal, Sopen, and Sshort. The Sopen, Sshort parameters for the power grid are processed to obtain the S parameter matrix for the power grid. It is assumed that this S parameter matrix is symmetric and reciprocal. Therefore, $S_{11\text{grid}} = S_{22\text{grid}}$ and $S_{21\text{grid}} = S_{22\text{grid}}$. Following formulae are used for the grid S parameters:

$$S_{11\text{grid}} = \frac{S_{\text{open}} + S_{\text{short}}}{2} + S_{\text{open}} - S_{\text{short}}$$
$$S_{21\text{grid}} = \sqrt{(S_{11\text{grid}} - 1) \times (S_{11\text{grid}} - S_{\text{open}})}$$

A simple RLGC model for the power grid is extracted from the measured S parameters as shown in Figure 6.

**Figure 6 On-die power grid model extraction**
For this small structure, the following values are obtained for the power grid: 
R_{\text{grid}}=250 \text{mOhms}, L_{\text{grid}}=20 \text{pH}, C_{\text{grid}}=1.3 \text{pF}, G_{\text{grid}}=1e^{-5} \text{S}. This model showed a good fit up to several GHz, and beyond 10GHz a higher order model will be required. Also, frequency dependent RLGC model is created and fitted with the measurement data, for higher frequency accuracy.

**Correlation and Tradeoffs**

External tool RH_PG results are compared with the measurements. The tool extracts R, C parasitics for the grid. For open circuit case, RC equivalent circuit is extracted. Figure 7 shows the open circuit Z11 comparison for the power grid. The simulated Z11 values are higher than measured, but it shows a similar trend in up to 10GHz. Open circuit Z11 corresponds to equivalent capacitance and equivalent conductance of the grid. Based on the correlation, the simulated equivalent power grid capacitance is smaller than measured.

Figure 8 shows the simulated and measured Z11 comparison for the short circuit power grid. The Resistance only model has been extracted for simulations. The tool does not use inductance (L) elements for the power grid in the reduced netlist for the grid. At low frequencies it is showing a reasonable match, but at high frequencies (>1GHz) measured Z11 is higher than simulated. The short circuit Z11 corresponds to the equivalent resistance and inductance of the grid. The tool does not show the inductive effects at higher frequencies.

![Figure 7 Z11 Correlation for open circuit power grid](image-url)
Overall, the RH_PG tool is user friendly and can take the grid layout information as input. It can extract the grid parasitics in a reasonable amount of time. It does not take into account the equivalent L and G for the power grid in the reduced netlist for the grid model. User needs to make the accuracy-performance tradeoff with the tool usage. This tool can be used to make preliminary estimation for the power grid parasitics. The generated models can be enhanced by the user to make them more accurate.

**Decap Model Extraction**

As mentioned earlier, S parameters for the grid (S11grid and S21grid) are obtained from the open circuit and short circuit measurements. Then, the S parameters for the decap are extracted from the following formula:

\[
S_{11\text{decap}} = \frac{S_{11\text{tot}} - S_{11\text{grid}}}{(S_{21\text{grid}}^2) - (S_{11\text{grid}}^2) + S_{11\text{grid}} S_{11\text{tot}}}
\]

A simple decap model is generated to have R, C and Leakage, as shown in Figure 10. The following values are extracted for the decap model: Rdie = 100kΩ, Cdie = 3pF, Rleakage = 100Ω. It showed a good correlation with S parameters to about 10GHz, as shown in Figure 9.

The power grid and the detailed decap models are then used for the system level simulations. The sensitivity of the Rdie and Cdie to system level performance is determined.
Figure 9 On-die capacitor model extraction

Conclusions

It is essential to develop frequency dependent accurate models for the on-die PDN, when using it in system simulations. On-die power grid and decap is characterized for the special test-structure. The grid parasitics play important role in the system performance. The grid model and the decap model are established. The correlation is performed with the external tool RH_PG. It shows a similar trend with the measurements. The model generated by this tool is a preliminary estimate and some enhancements will be required for using it in the system.

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Bibliography/References