System level PDN analysis enhancement including I/O Subsystem Noise modeling

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Abstract

- Power supply noise and its induced jitter are the dominant contributors to system performance degradation and even system malfunction. Occasionally the reciprocal phenomenon occurs when slightly phase challenged clocked data patterns can induce cumulative noise on independent, carefully designed critical supplies. The challenge in uncovering the root cause of a system malfunction due to this latter phenomenon comes from the fact that despite their acknowledged interdependency Power Integrity and Signal Integrity challenges are usually tackled independently as uniquely identifiable and verifiable entities.

- The methodology proposed here provides a bridge between power integrity of a PLL as influenced by the large current swings of a DDR PDN and large signal swings of a DDR signal interface. Correlation with PG noise and jitter lab measurements confirms that our Sentinel SSO based methodology is critically instrumental in intercepting noise due to independently supplied IO cells switching activity severely impacting dedicated VDDPLL and VSSPLL. Our system level workbench encompassing die, package and PCB interconnects exposed the impact of the capacitive and mutual coupling enabled outside the die on the PLL supply. It also allowed selecting the best (package rerouting in this case) solution for PLL supply noise reduction.
Outline

System level PDN overview
  • System level PG noise deconstruction
  • Value proposition

PDN noise modelling enhancement
  • Drivers and goals
  • Design and environment
  • Executive Summary
  • Details of simulations setups and results

Conclusion
System level PDN overview

System level PG noise deconstruction:

1. Switching activity
   
   Direct mechanism:
   
   • Simultaneous switching of digital as well as analog cells generate transient current spikes and thus transient voltage drops $\Delta V = Z_{RLC} \Delta I$

   Indirect mechanism:
   
   • The analog and digital supplies are mutually and capacitive coupled
   • PG acting as current returns paths for switching signal nets

2. Resonances:
   
   • Parallel plate resonances - local maximum minima voltage peaks
   • RLC series resonances
Value proposition

- In the current PDN analysis methodology the coverage of the AC ripple voltage phenomenon is limited to digital switching activity causality. AC ripple voltage due to custom IO switching activity or analog clocks activity is not evaluated.

- Proposed methodology based on Sentinel SSO enables the simulation of the interaction between IO noise and PDN.
  - When transistor models are used for the IO buffers a 100ns simulation would take 64 hours.
  - Using a macro model for the IO buffer the simulation would take 24 minutes with similar results.

- Passive contributions from the core supply can also be included in the analysis.
Drivers and goals

• Accounting for PG noise sources that previously had not been taken into consideration.
  – Analyze a full chip IO system
  – Analyze the contribution DDR signal activity to PLL power integrity
  – Monitor the noise at the PLL metal1 pins due to coupling with the DDR and the chip (negligible), package and pcb.

• Ease of integration within design flow

• Productivity improvement since the setup can be used for DDR/SSO analysis as well as PLL/DDR system analysis.

• Possibility to quickly learn the basics of the tool

• Using co-analysis of chip-package-system to provide a more holistic view of noise at the detailed chip level.
Methodology

• CIOM, models were generated of all the I/O cell instances from the converted design files, by applying user specified stimulus and connecting the PKG/PCB model to the I/O cells.
• On-die P/G grid reduced SPICE model was generated from the physical design.
• The chip model is then integrated with the rest of the pkg and pcb models for the system.
• Transistor models for the DDR IO buffers were used in initial simulation to qualify the ciom models.
• Various pkg/pcb models were then used to simulate the changes in noise seen by the PLL due to the DDR.
Executive summary

Noise from DDR signal activity on PLL PG supply quantified:

• Noise in the PDN that could not be found with any other tool/methodology currently deployed. We compared 3 existing package models that were mounted and measured on the same pcb. Sentinel confirmed the lab findings.

Setup:

• The project was setup quickly through a gui interface
• Three different package bonding models were extracted upon “soldering” the package design onto the PCB
• The channel included a full and compact package mounted on pcb model that accounted for all databit, address bit and control bit lines as well as for the 1.8V and 1.8PLL supplies coupling and for the characteristics of the system level GND
Current return path is different between DC/Low frequency and HF
Mutual coupling between VDDAPLL and BD5 and VSS wirebonds are dominant at HF
Capacitive coupling between VDDA PLL and VDD1.8 of the DDR23 is dominant at clock frequency
Current return paths are frequency dependent and are expected to be adding a distinctive noise component
Chip View

- Cells included in analysis/schematic interactively added/removed.

- The PLL supply, entirely separated from the 1.8V analog supply was included in the layout extraction.
- Good isolation between DDR_PLL_VDDA and DDR_DATA IOs.
Results

Using macro models for IO with accurate PI/SI properties allowed for fast computation times with similar results to full xtor level simulations. (24 minutes vs. 64 hours)

Time domain waveforms comparison of VDDA PLL noise

Based on run times criteria, further comparisons were based on ciom models.
Results

Time domain comparison on VDDA PLL noise

- VDDPLL noise: given the separation of the supplies on die, the VDDPLL noise captured at the SOC pin is entirely due to the coupling in the package and on the pcb

Frequency domain comparison on VDDA PLL and VSS PLL noise

- FFT shows that VDDPLL carries 800MHz the clock signature
Lab correlation

• DDR READ/WRITE Transactions
  • All IOs toggling 1->0 and 0->1, 4 bursts of 1K DDR transaction
  • SoC: high strength and high slew late (DRV1 = 1, DRV0 = 1, SL0 = 1), no ODT
  • DRAM: high strength (100%), no ODT
  • 5 parts were measured

Original package

DDR_PLL-VSSA connected to chip VSS bar

Write Buffer, 2us/div
Conclusion

- We explored a flow traditionally used for system level PI/SI co-analysis on a parallel interface to include the supply noise effects seen by a PLL device at the metal1 level due to this activity.

- Noise in the PDN that could not be found with any other tool/methodology currently deployed was analyzed and quantified.

- Our methodology demonstrates the importance of the system level interactions: although the switching data bit lines are only infinitesimally coupled on die to the dedicated VDDPLL they are strongly coupled to the VDDPLL on pkg/pcb and in the package.

- The methodology proposed here allowed choosing the best option between 3 different package options.

- Our methodology captured the PG noise coupling mechanism dependence with the frequency.