ANSYS®

COMPREHENSIVE LAYOUT-BASED ON-CHIP AND CHIP-PACKAGE-SYSTEM ESD SIGN-OFF SOLUTION

Location: EOS/ESD Symposium, Westin La Paloma, Tucson, AZ
Date: September 11, 2014
Time: 8:30 a.m. - 4:30 p.m.
Cost: $525.00

This tutorial will cover chip-package-system ESD analysis with ANSYS-Apache tool suites. It covers lecture and demonstrations of how to perform a systematic chip-level static and dynamic ESD analysis using PathFinder, a robust silicon proven solution that has been certified by several semiconductor foundries. We will review identification of HBM/MM/CDM on-chip ESD failures and root-cause analysis using PathFinder. We will also review how system-level ESD analysis is performed with ANSYS HFSS and ANSYS SIwave platforms using chip level ESD models generated by PathFinder.

AGENDA:

The tutorial is divided into 3 sections covering in-depth details on how to address ESD requirements challenges.

Chip-level Static ESD Analysis
8:30 a.m.- 12:00 p.m. w/ 30min. break

You will learn how to setup and run a full-chip layout-based ESD analysis on Analog Mixed-Signal (AMS) design and System-on-Chip (SoC) that includes:

- Comprehensive layout based pin-to-pin ESD connectivity checks
- Pin-to-pin resistance checks with root-cause analysis
- Interconnect failure analysis to ensure robustness of on-chip ESD network
- Case-studies showcasing ESD failures and how they were uncovered with PathFinder

Lnnch
12:00 p.m.- 1:00 p.m.

Dynamic ESD Analysis
1:00 p.m.- 2:30 p.m.

You will learn how to perform IP-level transient ESD simulation that includes:

- IP level transient ESD simulation setup to aid failure analysis
- Transient ESD behavior diagnosis and analysis including modeling of die-level metal grid, substrate network and well-diodes, effective capacitance of the package, and pogo pin
- Case studies with HBM and CDM failures uncovered with PathFinder

Break
2:30 p.m.- 3:00 p.m.

System-level ESD Analysis
3:00 p.m.- 4:30 p.m.

You will learn how to perform system-level ESD simulation that includes:

- Chip ESD Compact Model (CECM) generation using PathFinder for system level ESD analysis
- Full-wave models generation of ESD gun, ESD protection devices, PCB wires/vias and connectors using HFSS and SIwave
- Comprehensive chip-package-system (CPS) based dynamic ESD simulation addressing IEC61000-4-2 testing and correlation to silicon measurement

REGISTRATION:

Register at http://esda.org/symposiaEOS-ESD.html

1. Complete the personal and registration questions
2. Choose OPTION 3 - SYMPOSIUM PLUS TUTORIALS OR SEMINARS
3. Under Thursday, September 11, select ANSYS-Apache Comprehensive Layout-Based On-Chip and Chip-Package-System ESD Sign-off Solution
4. Complete your registration

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