Challenges for Power, Signal, and Reliability Verification on 3D-IC/Silicon Interposer Designs

Norman Chang, VP and Sr. Product Strategist
Outline

• 3D-IC/Silicon Interposer Trend
• Multi-die Power Integrity Need
• Stacked Die Reliability Concerns
• Wide-I/O Signal Integrity Issues
• Summary
3D-IC/Silicon Interposer Trend

- 3D-IC & Silicon Interposer competitive advantages
- Higher performance, lower power, and reduced form factor
- Optimal cost structure, reducing porting/design cost
- Better time-to-market through easier and faster integration
Why Silicon Interposer?

• Small form factor with economical packaging
  – Driven by continuous demand of smaller/faster/higher design integration at a cheaper cost
  – Enhanced system performance (higher bandwidth and lower power) via high density interconnect

• High-performance wide-I/O connections to RAMs
  – Shorten interconnection from chip-to-chip via SiI
  – Low driver/receiver power: Interposer C << package C

• Good fit to silicon process technology
  – TSV independent of technology nodes, decoupled from platform technology
  – Lower cost organic substrate
Challenges of Silicon Interposer Design

- Multi-die logic partition for floor plan and P&R
- Test methodology
- TSV-aware DRC/LVS
- TSV extraction
- **Power integrity**
  - Early/sign-off analysis
- **Reliability integrity**
  - Power/thermal/stress/EM/ESD
- **Signal integrity**
  - Wide-I/O jitter analysis
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Stacked Die Power Integrity Analysis

- Shared P/G network for Silicon Interposer designs calls for multi-die power integrity analysis
- Simultaneous switching activity on multi-die impacts IR/DvD on individual die
Concurrent Multi-die Voltage Drop Analysis

- Input multi-die design and corresponding process data (can be of different technologies), all at once
- Impact from shared P/G nets and decap in interposer die can be factored into memory and logic die
CPM-based Multi-die IR/DvD Analysis

- Most suitable when one die is external without the complete design database
- Chip Power Model (CPM™) is a die model with R/L/C network and current profile, generated by RedHawk™ or Totem™
- Enables simple hand-off and fast turn-around-time

Logic Die
LEF/DEF, N65 iRCX

Silicon Interposer
LEF/DEF, N65 iRCX

CPM

Memory Die
LEF/DEF, N40 iRCX

RedHawk

Totem

Package Netlist
• Connected in a face2back manner
• “Top die” connects to “package” through “bottom die”
• Bottom die PDN contains TSVs that connect its M1 to back-side metal, which connects to top die using “copper pillars”
• RLCK model of package used
3D-IC Test Case Description

Layout view of both die in concurrent mode

Model of top die hooked to bottom die layout
Voltage drops on two die in two cases:

<table>
<thead>
<tr>
<th></th>
<th>Case A</th>
<th>Case B</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Top Die</td>
<td>1.00</td>
<td>1.00</td>
</tr>
<tr>
<td>Power Bottom Die</td>
<td>0.33</td>
<td>0.33</td>
</tr>
<tr>
<td>Voltage Drop Top Die</td>
<td>10.94</td>
<td>11.91</td>
</tr>
<tr>
<td>Voltage Drop Bottom Die</td>
<td>4.67</td>
<td>3.7</td>
</tr>
<tr>
<td>GND bounce Top Die</td>
<td>5.03</td>
<td>6.57</td>
</tr>
<tr>
<td>GND bounce Bottom Die</td>
<td>2.31</td>
<td>1.00</td>
</tr>
</tbody>
</table>

**Case A:** top half of the top die is active

**Case B:** left half of the top die is active

Bottom Die is affected by operation of the Top Die!

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Multi-die Reliability Concerns

- Strong power-thermal interaction, especially on leakage power
- Thermal distribution more complicated due to multi-die interaction
- Thermal-induced stress more severe due to different process technologies
- Temperature-dependent EM limit changes significantly at 28nm or below technologies
- ESD is worse or similar on HBM/CDM models
Power-Thermal (PT) Loop

Through Co-analysis:
- Power/Thermal Convergence
- Thermal Run-away

Note: Total power and maximum temperature on chip
Power-Thermal Convergence Using Sentinel-TI

- Ambient Temperature
  - Still Air or Air Speed
- External Heat Sink
- Molding
- Die
- Die Attach
- Ambient Temperature
- Still Air or Air Speed
- Substrate
- PCB
- Wire
- Solder
- HS Attach
- Die Attach
- Mask
- Updated Temperature
- Updated Power
- CTM from RedHawk/Totem
  Look-up power map from temperature map
Test Case with Silicon Interposer

2D TIS (Through Interposer Stack)

Tier 1 (Si Interposer) Face Up

Tier 2 (Chip 1) Face Down

Tier 2 (Chip 2) Face Down

Substrate

feedthru net (chip IOs)

TSV

RDL routing

inter net

Substrate

Backside metal

Package

front_side ubump

back_side ubump

Stacked Silicon Technology
(courtesy of Xilinx paper)

TSMC Ref 12 Test Case

Apache Design, a subsidiary of ANSYS
Thermal Analysis of 2.5D Silicon Interposer Design

Memory Die

Logic Die

Power Density

Temperature

Memory die’s thermal map is affected by Logic die of higher power (0.12W from logic vs. 0.005W from memory)
Example of Power Density Map and Layer Thermal Responses with CTM-based Flow
3D-IC Thermal Analysis Flow: 
CTM-based Power-Thermal Co-analysis

CTM: Chip Thermal Model
Temp-dependent power database

IC Power Integrity Analysis

RedHawk

IC DESIGN

CTM Generation

Power update
R Extraction
EM limit update

Sentinel-TI

Thermal Co-analysis

Thermal/Stress Analysis

Package Design (mcm, sip)

System Thermal Tools

JA/JB/JC Delphi
Power Map

JA/JB/JC Delphi
Power Map

System
Thermal
Tools

Thermal Profile

Icepak

Memory
Substrate
SoC
Substrate
Si Interposer
Substrate
Package
TSV
front_side
ubump
back_side 
ubump
feedthru net 
(chip IOs) inter 
net
Backside metal
RDL routing

JA/JB/JC Delphi
Power Map
Deformation/Stress in Packages

- Where does deformation/stress come from?
  - Differential thermal expansion due to on-chip temperature increase
  - Silicon chips have very low thermal expansion coefficients and are pushed and pulled by surrounding components

Expansion movements

<table>
<thead>
<tr>
<th>Component</th>
<th>Expansion Coefficient</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mold</td>
<td>2.6 ppm/C</td>
</tr>
<tr>
<td>Die</td>
<td>12.7 ppm/C</td>
</tr>
<tr>
<td>Substrate</td>
<td>12.4 ppm/C</td>
</tr>
<tr>
<td>Board</td>
<td>17.4 ppm/C</td>
</tr>
</tbody>
</table>

ppm = mm/mm x 10^{-6}
Multi-die Stress Analysis

- Higher stress on logic die due to higher power dissipation and temperature
- Resulting in more thermal to relative Silicon Interposer

\[ \text{Tmax} = 55.95 \, ^\circ\text{C} \]
\[ \text{Tmax} = 58.70 \, ^\circ\text{C} \]
Thermal Impact on Electromigration

Black’s equation for Mean-Time-To-Failure (MTTF)

- Electromigration: transport of metal due to high current flow
- Black’s Equation

\[ MTTF = \frac{A}{J_{\text{max}}^2} \exp\left(\frac{E_a}{k_B T_m}\right) \]

- \( T_m \) - Temp of Metal Wire
- \( J_{\text{max}} \) - Current Density Limit

\( T \uparrow \text{ J} \downarrow \) for same MTTF
Thermal Aware Power and Signal EM

Power EM Maps

Traditional Analysis constant “high” T

Thermal-aware Analysis based on “actual” T

Signal EM Thermal-aware results

Thermal-aware EM analysis avoids false violations and over-design
ESD Comparison between 3D-IC / Silicon Interposer Design and Single Die Package

- **3D-IC**
  - HBM (better due to TSV slows down the discharging rate but can be worse on the condition below)
  - CDM (slightly worse due to more charges)

- **2.5D Silicon Interposer**
  - HBM (similar due to common TSV path)
  - CDM (worse due to larger package)
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Wide-I/O Example: SoC + RAM on Interposer

• Chips face down, Interposer face up

• Interposer connects:
  – To chip μbumps
  – Among μbumps and TSVs via front-side wiring
  – To package via TSVs + C4 solder balls on back-side
  – Parallel bus channel (1K-8K bits)
Modeling Wide-I/O Jitter Through Interposer

- SoC drivers and receivers + core noise
- Interposer rails, signals nets, passives
- IBIS or other RAM model
- Stimulus
Jitter on Sil Parallel Wide-I/O Bus Example

aggressor: m_data2[4]

victim: m_data2[3]
Summary

• Increasing number of shared P/G ports require analysis of the entire 3D-IC (multi-die, package) for accurate power integrity

• Concurrent simulation method or CPM-based analysis method is possible due to availability of design data

• Reliability issues, including power/thermal/stress/EM/ESD are getting more serious for 3D-IC or Silicon Interposer designs

• Wide-I/O with Silicon Interposer will likely become a major platform for high performance logic<->memory designs, and channel jitter analysis is much needed