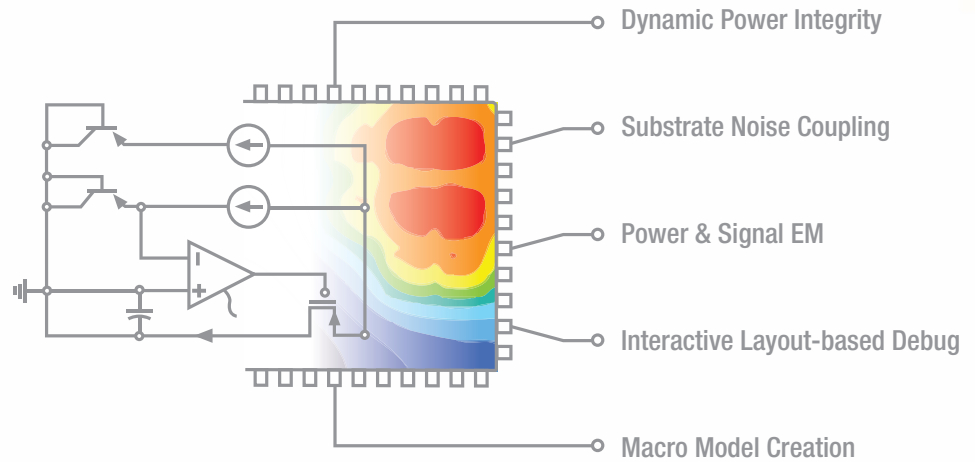


Totem™-MMX

Analog / Mixed-signal Power, Noise, and Reliability Solution

Totem-MMX is a transistor-level power/ground noise analysis and verification solution addressing static and dynamic power integrity needs from early stage in the design to sign-off validation. It addresses the verification of IPs designed using full-custom or semi-custom techniques for both analog and mixed-signal designs. Totem enables designers to verify power grid connection problems, identify high voltage drop causing mechanisms, and isolate electro-migration bottlenecks.



KEY CAPABILITIES

- Delivers full-chip capacity with SPICE-level accuracy for transient power/ground noise analysis
- Concurrently analyzes noise propagation through power delivery network, substrate network, and package/PCB parasitics
- Provides built-in extraction and simulation engine with fast incremental and "what-if" analysis
- Enables grid weakness check, "hot spot" root cause identification, and design fix exploration, delivering significant time savings and productivity enhancements
- Layout-driven analysis integrated with existing analog design environment
- Ability to generate models for hierarchical full-chip and system-level simulation
- Performs power and signal electro-migration signoff supporting industry standard and advanced process technology EM limit

Overview

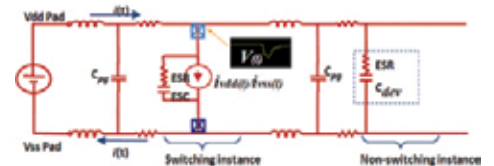
Totem-MMX is a comprehensive solution that incorporates transistor-level noise injection, parasitic extraction, package modeling, dynamic analysis, and design debug in a single-flow environment to enable analog/mixed-signal designers to mitigate design failure risks and reduce the product cost.



Accuracy and Capacity

Totem-MMX incorporates transistor-level modeling with voltage de-rated switching current techniques and SPICE-accurate decoupling capacitance (decap) extraction for highly accurate power noise analysis. It pre-characterizes the circuit using the SPICE netlist, device models and input vector set, and is simulated using industry standard SPICE simulators. The characterization process captures switching current waveforms for all switching transistors as a function of voltage for various operating conditions, as well as their intentional and intrinsic capacitance. It also considers the impact of package and

board RLC through the support of broadband S-parameter package and PCB models.

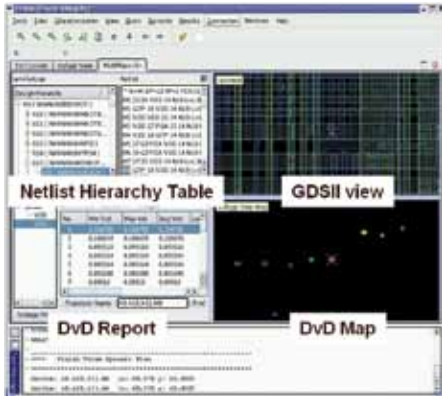


Circuit modeling for PG noise simulation

Totem-MMX delivers the capacity required for standalone DRAM, Flash, and CMOS image sensors, as well as embedded memory macros.

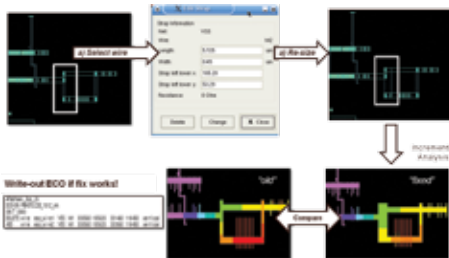
Layout-based Unified Analysis and Debugging Environment

Totem-MMX provides advanced viewing, debugging and fixing capabilities to effectively analyze and optimize full-custom designs. Its layout-driven interface is integrated with existing analog design environment and supports cross-probing of power noise violations with the industry standard layout schematic tools, as well as interactively analyze the fixes made in the design.



Multi-frame GUI – Cross check layout, netlist and analysis report on single page

The powerful ‘what-if’ capability allows designers to quickly verify a fix before committing to the layout. Fixes such as decap insertion and addition or removal of metal or via can be verified using incremental extraction and re-analysis to ensure that the proposed change does indeed fix the violation.



“What-if” analysis for upsizing wire width to fix IR drop

IP Creation and SoC-level Analysis

Totem-MMX can analyze and validate power noise issues at the IP level and generate a model of that IP that can be used for SoC or top-level power noise analysis. It incorporates

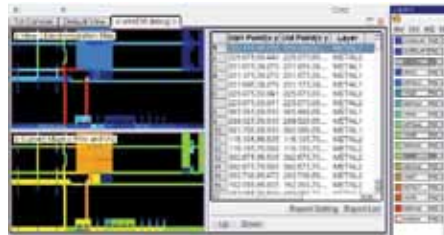
top-level connectivity and noise coupling scenario for block/IP-level analysis. Once validated, the designer can generate a detailed model capturing layout and circuit behavior of the IP.

IP model generated by Totem-MMX, Custom Macro Model (CMM™), captures different operating states such as “read” and “write” with its associated current and other parameters. It also enables designers to embed constraints such as maximum voltage drop allowance on transistors or a metal layer for top-level verification.

For multi-company IP integration, Totem-MMX provides various levels of IP encryption to protect the intellectual property of the circuitry. It delivers an optimized model for quick top-level analysis, while preserving the overall integrity and without compromising its accuracy.

Power and Signal Reliability Analysis

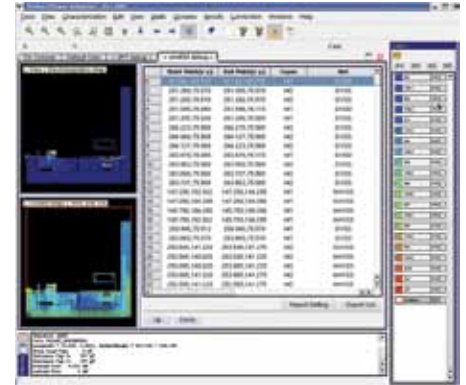
Totem-MMX provides a single platform for power rail and signal interconnect electromigration (EM) analyses. Power EM is performed as part of static or dynamic analysis. It supports EM limit for 65/45/28nm processes and provides checks for average, RMS and peak current densities. The EM results are easily checked and analyzed in the layout-based environment.



Integrated views of EM result table and violation

Signal EM analysis is performed for average, RMS, and peak current densities in all signal wires and vias. It supports unified run with separate uni-directional and bi-directional current analysis. Totem-MMX either estimates the current based on design parameter and user input or imports the current based on actual SPICE simulation. Totem-MMX analyzes

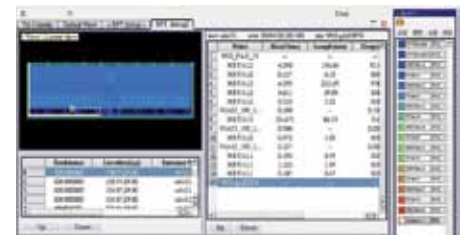
Signal EM checks on flattened transistor-level designs as well as on block-level inter-cells for embedded digital blocks. Its layout-based GUI with cross probing capabilities provides easy to use and robust debugging including detailed violation reports with current values and their direction.



Signal EM debugging – Searches shortest path of resistance

Connectivity Weakness Exploration

Totem-MMX verifies grid connectivity issues, such as missing vias and weakly connected devices. These connectivity issues can be debugged using the GUI and textual reports. Totem-MMX’s network topology analysis provides insights into routing issues that can cause voltage drop hot-spots or current congestions in the design. The shortest electrical path from the voltage supply pads to every transistor is provided as an overlay on the design layout allowing one to identify the bottleneck segments.



Integrated views of transistor pin resistance and its minimum resistance path