The Extraction and Measurement of On-Die Impedance for Power Delivery Analysis

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Abstract

Power delivery system noise, current and impedance are the key performance factors for successful chipsets/CPUs design. Power delivery noise is significantly affected by on-die impedance and current, i.e., on-die power grid equivalent resistance (Rdie), capacitance (Cdie), and Icc(t). Rdie and Cdie have been challenging in pre-silicon extraction and post-silicon measurement. This paper focuses on Rdie and Cdie extraction and silicon correlation. We carried out Rdie and Cdie extraction comparison study for Intel products that contain several PHY blocks by using home-brew flow, a commercial tool, and lab measurement, to achieve good correlation. The work boosts our confidence in the accuracies of internal flow and commercial tool and therefore facilitates the adoption of the commercial tool to greatly improve die grid modeling effort.

I. Introduction

Power delivery becomes a big issue in the design of today's microprocessor, chipsets, communication chips, and other semiconductor products. The market demand for higher speed, more functions, and lower power consumption results in the significant increase in operating frequency and the number of transistors, and the decrease of voltage. The consequent large current and low voltage necessitate a low-impedance path from the power supply to the die. Low-impedance in power delivery loop reduces not only DC IR voltage drop, but also power delivery noise. This is critical in today's low voltage and large current silicon design, especially for the circuits with power management features and lower active Vcc margins, such as some IO (Input/Output) analog circuitry. To save power consumption, circuits like PCIe will be powered down during low idle state; when several circuits power on again, potential large di/dt current can generate excessive supply noise which can cause signal timing issue or even functional failure. Hence, power integrity should be ensured so that power delivery droop/noise can be reasonably small to meet more stringent targets. As a part of the low-impedance power delivery network, on-die low impedance means low resistance Rdie and high capacitance Cdie. New technology requirements even push the on-die impedance into the order of milliohm or less. Accurate modeling of Rdie and Cdie is essential to this effort.

The accuracy of die grid modeling is important in better prediction of voltage droop/noise, silicon decap quantity, package decap type/quantity and package power/ground planes design, and even IO lane-to-lane staggering control. These can alleviate overdesign or underdesign in silicon and package which results in good quality and cost reduction, and avoids design reiteration. Furthermore, in the fast-paced IT market nowadays, a modeling flow/tool possessing both accuracy and high efficiency/capacity is even more robust and in demand. It can shorten turnaround time so that the silicon/package designers can try different design options and do analysis to optimize designs quickly. This helps to shorten design to market time with high-performance and low-cost products.

The team developed the home-brew On-Die PDA toolset about 4 years ago [1] before the commercial solution was widely adopted in the design team. Since then, it has been used to deliver die grid model for several Intel products. To validate the two pre-silicon extraction toolsets, we correlated their results with lab measurement. Good correlation was observed in core Cdie [2][3]. For continuation, this paper extended to Rdie correlation for core/IOs and Cdie correlation for IOs, both of which have not been found in publications. We applied the two extraction flows to extract lumped RdieCdie for several PHY blocks as well as core. VNA (Vector Network Analyzer) was used in lab to measure lumped RdieCdie. Reasonably good correlation among the three approaches was observed.

II. Internal Tool: On-Die PDA (Power Delivery Analysis)

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On-Die PDA is an internal extraction/simulation tool [1][2] to generate on-die power delivery models, i.e. Rdie, Cdie, and Icc(t). Cdie extraction was described in detail in [1]. After Cdie calculation and power/ground grid extraction, the entire extracted Vcc/Vss network with all on-die decaps connected at their corresponding locations is plotted in Figure 1. By shorting all Vcc bumps together and shorting all Vss bumps together in a functional block, and running AC simulation, we can obtain the equivalent Rdie for this block.

III. Commercial Tool

The commercial toolset we used is developed **Error! Reference source not found.**for power integrity analysis solutions [4]. For IO, there are two types of tools: one is used to characterize IO circuitry, while the other to generate on-die models. When utilized together, they are capable of generating frequency-dependent on-die models for IO blocks. For core, another tool can be used to generate on-die models for core partitions. The on-die model extraction of the tools is based on the principle: transistors are modeled as current sources with ESR and ESC, decap cells are modeled as capacitors/ESR, and the power/ground grid is extracted as RLC network.

IV. VNA Lab Measurement

To measure the low impedance of power delivery network in frequency domain, we adopted a robust 2-port VNA metrology introduced [5]in 1999 [5]. The Device Under Test (DUT) was with die and package together. Package decoupling capacitors were removed to reduce the number of parameters in on-die impedance measurement. Probing was conducted at package probing pad due to the difficulty to probe directly at tiny silicon bumps. VNA testing yielded S-parameters for DUT, hence the impedance of DUT (Z_{DUT}). To extract RdieCdie, the assumption was made that the die and package could be modeled as the equivalent circuit in Figure 2, and curve-fitting technique was utilized [2][3].

V. Correlation Results

The above three approaches were applied to two Intel products. Table1 is for an IO interface from one product (Chip1) with post-silicon measurement unavailable yet. Table 2 and 3 are from another product (Chip2) which has lab measurement: the former is for IO, the latter is for core. The results from two simulation toolsets are close for both IO and core. The largest difference on Rdie is 20% and Cdie 17%. It also can be seen that, for Cdie, the extracted data agreed well with VNA lab data for both IO and core, with the max delta of 17%. However, for Rdie, bigger discrepancy was observed between extraction and lab measurement with VNA number about 7 times extraction number in the worst case. But note that the Rdie absolute value is quite small in this case.

Several factors might contribute to the discrepancies in RdieCdie correlation among the three techniques:

1. In real system, the equivalent Rdie and Cdie are functions of frequency, and they are not fixed numbers, so the lumped models of Rdie and Cdie with fixed values are definitely approximations. Besides, the model assumption for lab measurement in Figure 2 is highly simplified.
2. In lab measurement, when DC voltage is supplied to the silicon, the internal circuit states were unknown. This cannot be simulated, thus affecting Cdie and Rdie correlation. If the circuits were to be properly initialized and put into known state, correlation could have been better.
3. The lab measurement may not be very accurate, especially when measuring small Rdie for a power domain with big die area. The probing technique and the chosen port location affect measurement results. Package testing point should be properly designed and the relative locations of probes should be studied.
4. Curve-fitting scheme can cause discrepancy between simulated data and original data, especially when Rdie is small (like several miliohms), the delta can be big, due to the big range of the impedance curves. Highly zooming in the valley of the impedance curve is needed for proper Rdie fitting.
5. In On-Die PDA flow, curve-fitting scheme was used to extract RdieCdie, so the accuracy is also affected by package model accuracy. More accurate package model will help.
6. The Cdie from commercial tool is equivalent Cdie from AC simulation, but On-Die PDA obtains Cdie by summing up all capacitance components. The internal flow can be improved to match commercial tool.
7. In the two extraction tools, the assumption that all Vcc bumps are shorted and all Vss bumps are shorted is also a simplified one, which usually results in smaller Rdie.
8. Only two typical skew chips were measured in the lab. More parts are needed to establish the statistic profile (the mean and standard deviation) of Rdie and Cdie.

Regarding the Rdie discrepancy of several times when Rdie is small, a study was conducted to investigate its impact to power delivery noise. In a spice simulation test case, at platform power delivery system, Rdie was swept from 1mΩ (close to Chip2 entire core Rdie)/15mΩ/30mΩ/60mΩ while the other parameters remained unchanged. The system-level impedance Z(f) profiles in Figure 3 show that, as Rdie increases, the impedance Z at the 1st peak resonance frequency decreases, but impedance at higher frequencies increases. Figure 4 demonstrates the power supply noise waveforms Vcc(t) with Vcc peak-to-peak (Vccp-p) recorded in Table 4. In this test case, Vccp-p seems not sensitive to Rdie for small Rdie. For example, when Rdie increases from 1 mΩ to 15 mΩ, Vccp-p only increases by 7%. For Chip2, platform-level simulations with core Rdie sweep showed that either 0.7 mΩ or 5 mΩ did not make significant difference in Vccp-p. Therefore, the Rdie difference between extraction and lab measurement is acceptable. However, this might not be a general rule. The Rdie discrepancy origin will be further investigated in future work.

Finally, the efficiencies of On-Die PDA and commercial tool are also compared. For an interface such as Chip2 IO or core, On-Die PDA usually took an engineer about two weeks to extract Rdie and Cdie, with most of time in manual work, such as data preparation and step-by-step operation. Commercial tool normally took one or two days in data preparation and then the runtime was about one day.

VI. Conclusions

In this work, on-die grid modeling comparisons were performed for core and IOs by using internal On-Die PDA flow, commercial tool, and VNA lab measurement. The validation revealed that similar accuracies were achieved among PDA and commercial solution. In commercial tool, the feature of frequency-dependent die model can be useful for what-if type of power delivery solution explorations. But need to sanity check the results for validity. On-Die PDA is free but requires manual intervention and simulations; strong dependency on circuit design environment which is constantly changing with product generations or project team specific setup; and complexity.

VII. References

[1] Jung S. Kang, Peter P. Jeng, Michael M. DeSmith, Ke W. Wang, “On-die Model Methodology and its Application to RHSL Chipset Product on P1263”, Internal conference paper, 2005.

[2] Yi-Feng Liu, Brian Wang, Mingming Xu, Xiaoping Liu, Jie Zhu Chen, Michael Desmith, “Correlation of On-Die Capacitance for Power Delivery Network”, EPEP, 2008.

[3] PCG Low Power Design (LPD) Team, “Correlation of Chip2 Cdie Between Measurement, Commercial Tool, and On-Die PDA (Internal Script)”, internal documentation, March 20, 2008.

[4] Emre Kulali, Evgeny Wasserman and Ji Zheng, “Chip Power Model - A New Methodology for System Power Integrity Analysis and Design”, IEEE EPEP, proceedings pp. 259-262, Oct. 29-31, 2007.

[5] Istvan Novak, “Probes and setup for measuring power-plane impedances with vector network analyzer”, DesignCon, 1999.

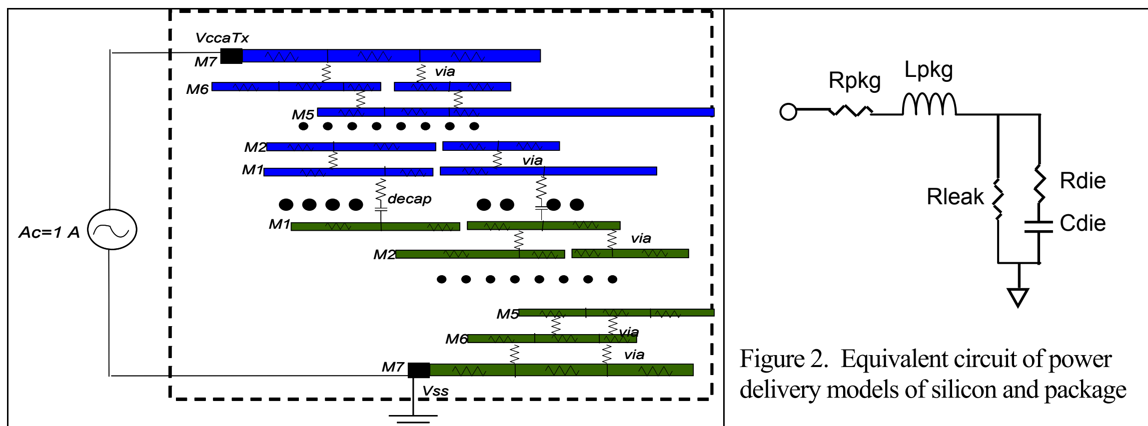

Figure 2. Equivalent circuit of power delivery models of silicon and package

Figure 1. The entire extracted on-die power delivery network

PHY block	Temperature	Commercial Tool		On-Die PDA		Difference	
		Rdie (Ω)	Cdie (pF)	Rdie (Ω)	Cdie (pF)	Rdie	Cdie
Blk1	50C	0.622	60.3	0.735	61.6	18%	2%
Blk2	110C	0.100	340.2	0.105	363.9	5%	7%
Blk3	50C	0.330	251.5	0.303	229.7	-8%	-9%
Blk4	50C	0.063	368.8	0.058	360.6	-8%	-2%

Note: Typical,1.1V. Difference: use commercial tool as reference.

Table 1. Comparison between two extraction flows for Chip1 IO

PHY block	Commercial Tool		On-Die PDA		Lab VNA msmt	
	Rdie (mΩ)	Cdie (nF)	Rdie (mΩ)	Cdie (nF)	Rdie (mΩ)	Cdie (nF)
Blk1	5.1	20.3	4.4	23.8	13.0	23.2
Blk2	6.0	20.4	5.5	22.8	15.0	21.0

Note: Typical, 1.0V, 25C

Table 2. Comparison among three techniques for Chip2 IO

Partition	Commercial Tool		On-Die PDA		Difference	
	Rdie (m Ω)	Cdie (nF)	Rdie (m Ω)	Cdie (nF)	Rdie	Cdie
Par1	13.61	2.7	10.87	2.56	-20%	-5%
Par2	22.69	2.23	18.8	2.08	-17%	-7%

Note: Difference: use commercial tool as reference.

Table 3a. Comparison between two extraction flows for Chip2 core partitions

Commercial Tool		Lab VNA msmt	
Rdie (m Ω)	Cdie (nF)	Rdie (m Ω)	Cdie (nF)
0.7	89.4	5	105

Note: Typical, 0.86V, 25C.

Table 3b. Comparison between two techniques for Chip2 entire core

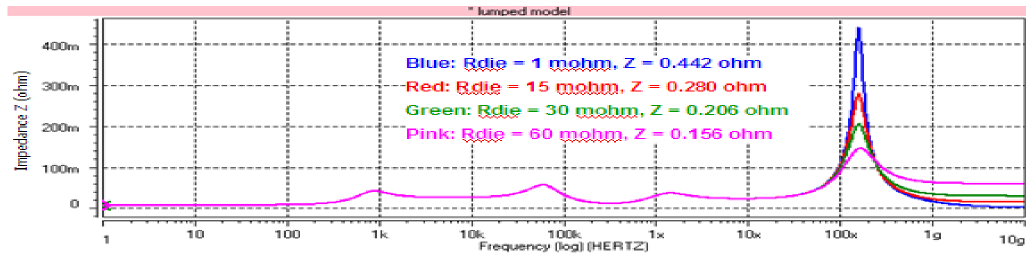

Figure 3. Platform-level power delivery impedance Z(f) profile for different Rdie

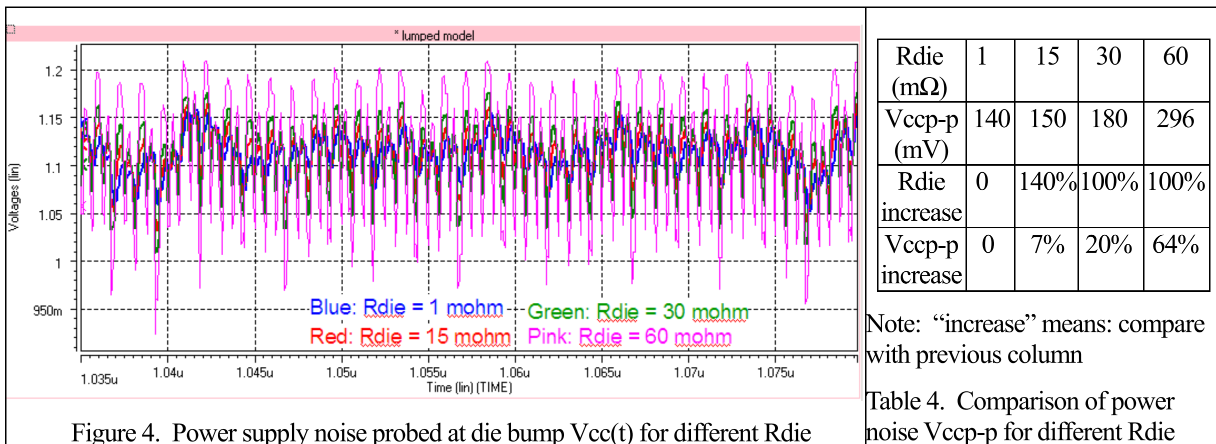

Figure 4. Power supply noise probed at die bump Vcc(t) for different Rdie

Rdie (mΩ)	1	15	30	60
Vccp-p (mV)	140	150	180	296
Rdie increase	0	140%	100%	100%
Vccp-p increase	0	7%	20%	64%

Note: "increase" means: compare with previous column

Table 4. Comparison of power noise Vccp-p for different Rdie