

# **Power Gate Design Optimization and Analysis with Silicon Correlation Results**

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# Disclaimer

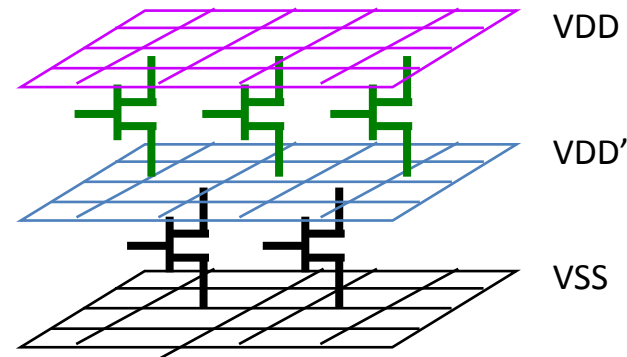
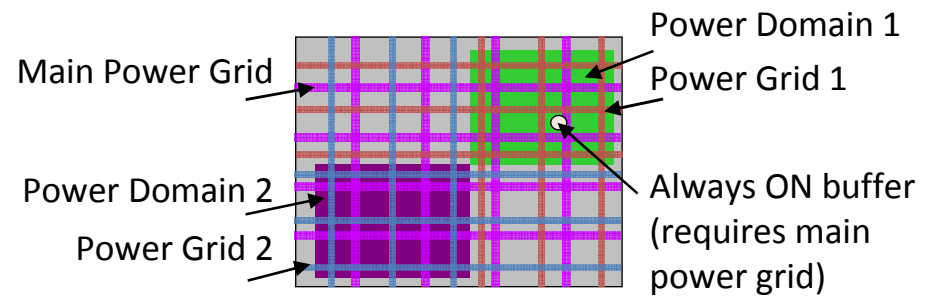
- **The flow results discussed have been simulated and are provided for informational purposes only. Results were derived using EDA software tool that run on an Intel's VLSI design. Any difference in VLSI design or software tool or configuration or flow may affect actual results.**

# Low-Power Design Trends

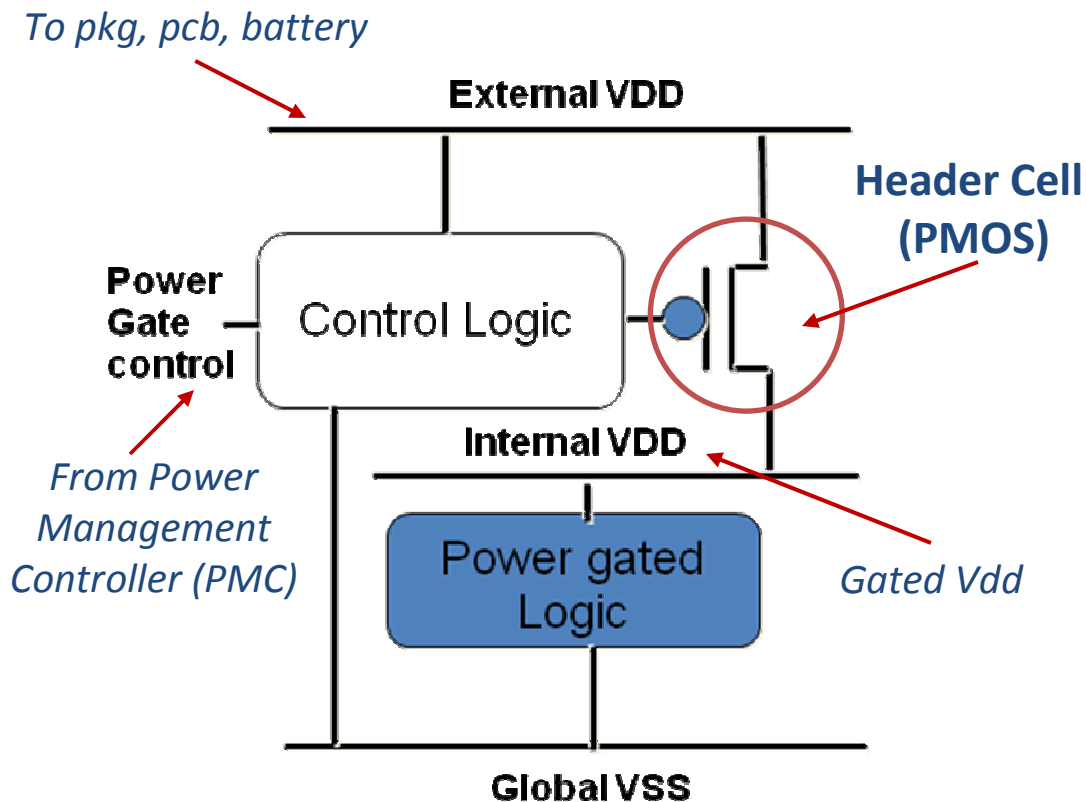
- **90nm**
  - Clock-gating
  - Multi-Vth, voltage islands
- **65/45nm**
  - Power-gating for standby power reduction
  - Decoupling capacitance optimization
  - Power-gated memories

# Power Delivery Network Challenges for Low Power Designs

- **Voltage islands require separate grids and bumps**
- **Power gating requires dedicated power grid and virtual Vdd**



# Distributed Power Gating Methodology

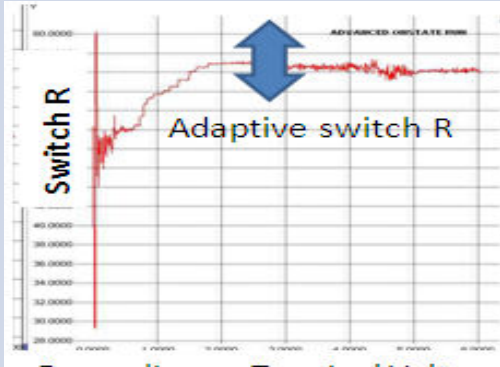


- Leakage accounts for nearly 50% of power
- Power gating results in significant reduction of stand-by power
- Control logic needs to ensure constant voltage for power and signal noise coupling immunity

# Early Design Decisions for Low Power and Leakage Management

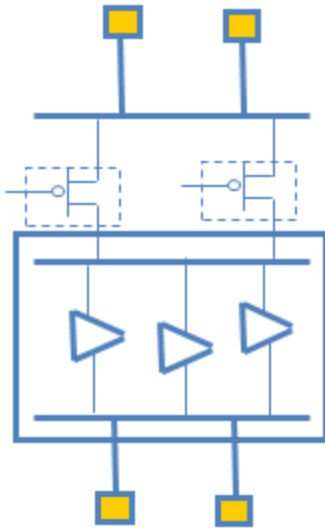
- **Size and placement of power gates**
  - Larger devices allow more current in on-state but increase leakage current in stand-by mode
  - Close proximity of switches to VDD bumps provide optimal current delivery and distribution
- **Ramp-up strategy**
  - Sudden demand of current (rush current) can induce large  $Ldi/dt$  noise
  - Longer ramp-up time can impact design performance

# Power Gate Switch Model Components

Mode	
<b>ON</b>	<ul style="list-style-type: none"><li>▪ Resistive model</li><li>▪ Function of terminal V</li><li>▪ With C, I(v)</li></ul>  <p>The graph shows the resistance of a switch over time. The y-axis is labeled 'Switch R' and ranges from 280,000 to 400,000. The x-axis represents time. A red curve starts at approximately 280,000, rises sharply to about 380,000, and then levels off. A blue double-headed arrow is positioned above the curve, pointing to the text 'Adaptive switch R'. The text 'ADVANCED OSCILLATE SIM' is visible in the top right corner of the graph area.</p>
<b>POWER UP, DOWN</b>	<ul style="list-style-type: none"><li>▪ Resistive model</li><li>▪ Function of terminal V</li><li>▪ Models off → on, on → off</li></ul>
<b>OFF</b>	<ul style="list-style-type: none"><li>▪ Current sink model</li><li>▪ Function of terminal V</li></ul>

# On-State Analysis

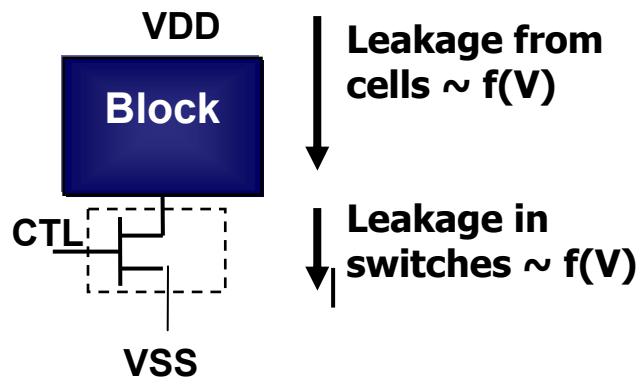
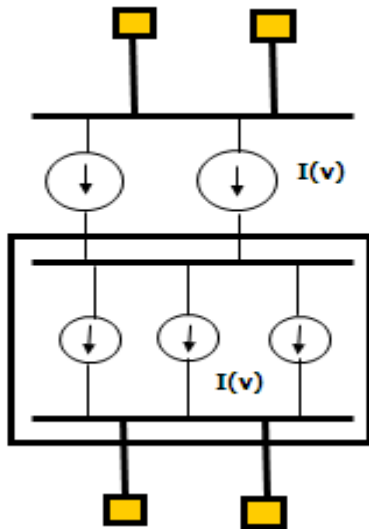
## On-state Model



- **Power gates create additional resistance paths**
- **Simulate for static and dynamic analysis with power gates fully “ON”**
- **Determine correctness of design, placement, and count**
- **Ensure power gating does not cause DvD/Timing degradation**

# Off-State Analysis

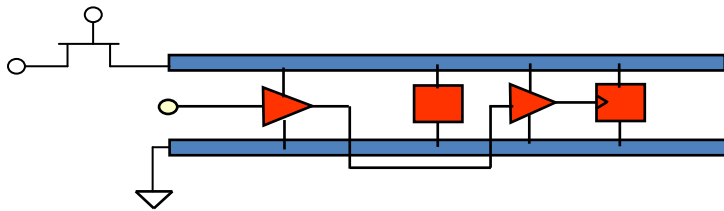
## Off-state Model



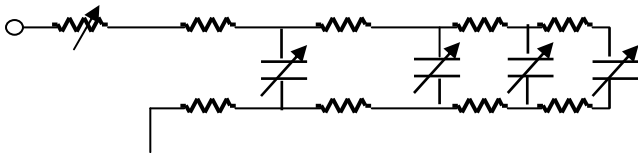
- Power gates block disrupt leakage current conduction in off-state
- Still leakage current path exists
- Leakage current  $\sim f(\text{node voltages, cell/switch leakage})$
- Header based designs have internal floating power nodes discharged.

# PowerUp/Down Analyses

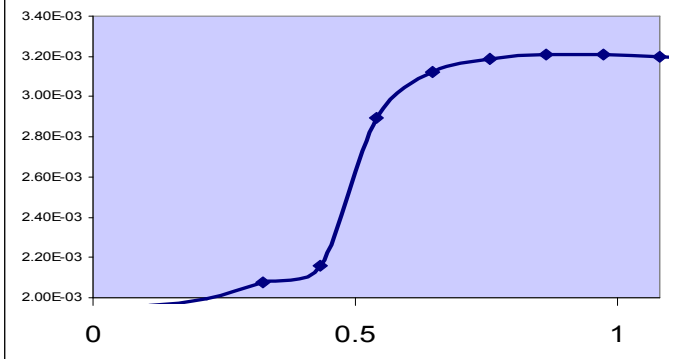
**Actual Circuit**



**Equivalent Circuit**



**Non-linear Capacitor Modeling**

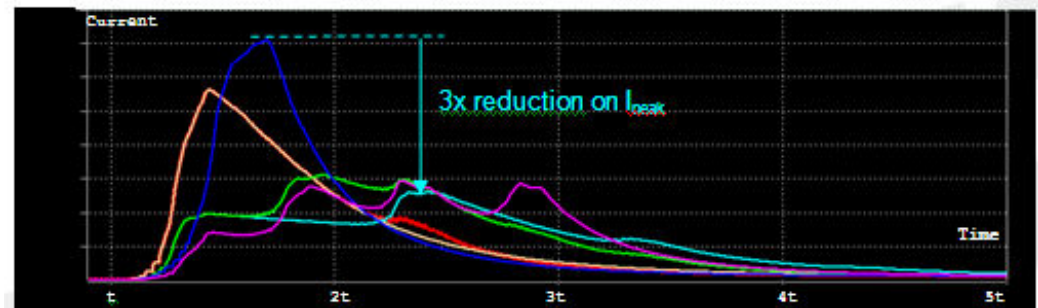


- Simulate for transition from off to on-state or vice-versa
- Start from off-state voltages at every node in the design
- Discharge internal ground nodes (for footers) and charge internal power nodes (for headers)
- Device intrinsic R, C and I function of voltage

# Early Switch Planning

## What-if Analysis

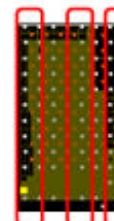
- Find the optimal combination of switch turn-on delays, count, and placement
- Tool functions (grid planning, switch placement, incremental analysis) used for early planning and prototyping



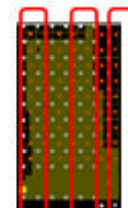
1) All switch on at  $t$



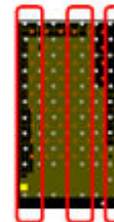
4) Gradual on of 5 columns with  $1t$  time delta



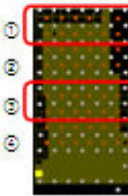
2) Alternating Column with  $1t$  time delta



5) Gradual on of 5 columns with  $0.5t$  time delta

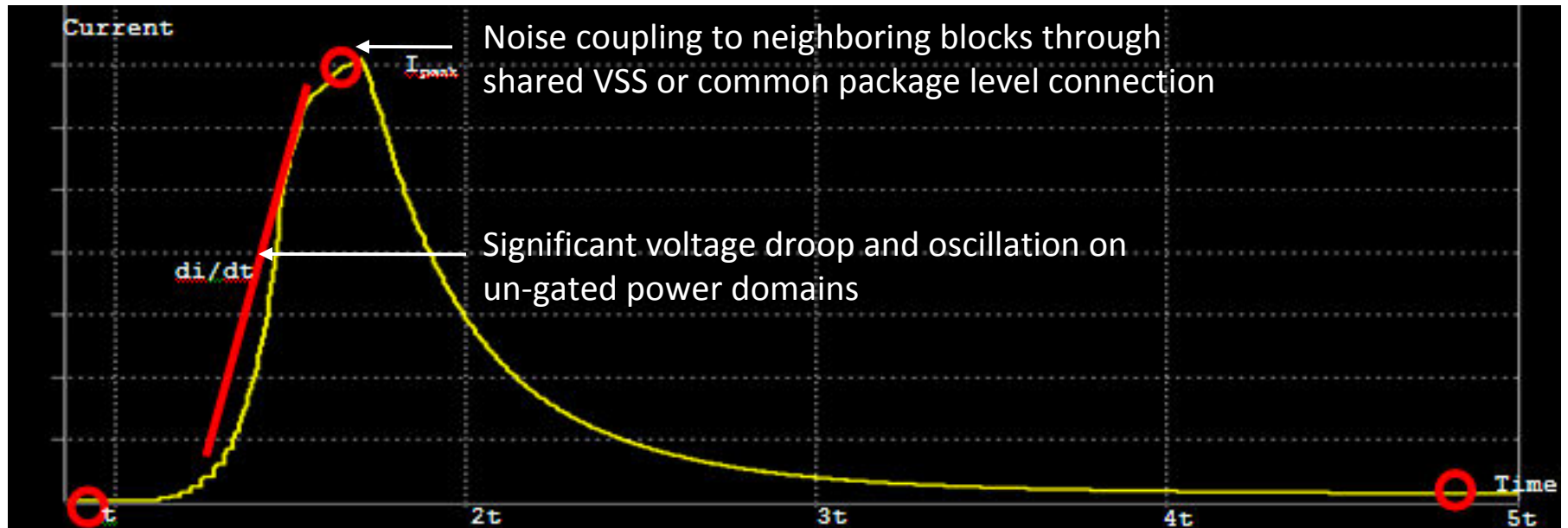


3) Alternating Column with  $4t$  time delta



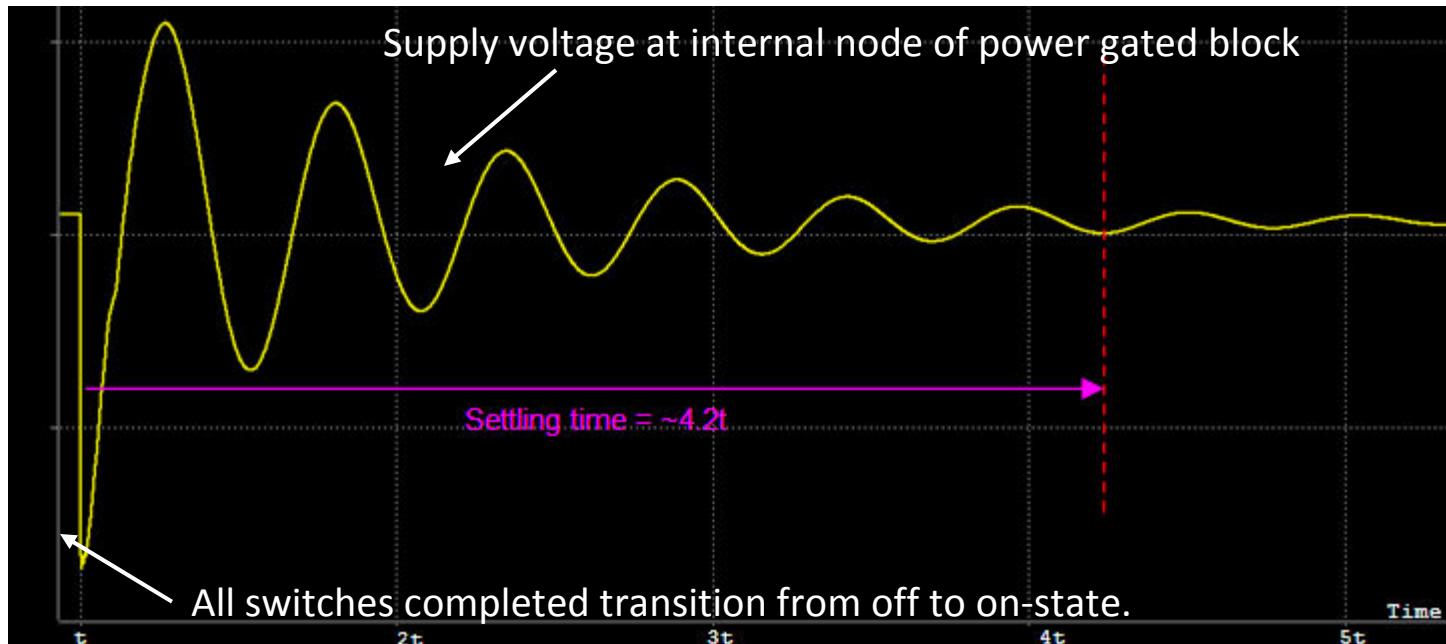
6) Gradual on of 4 rows with  $0.5t$  time delta

# Rush Current of Sudden Power-Up/Down



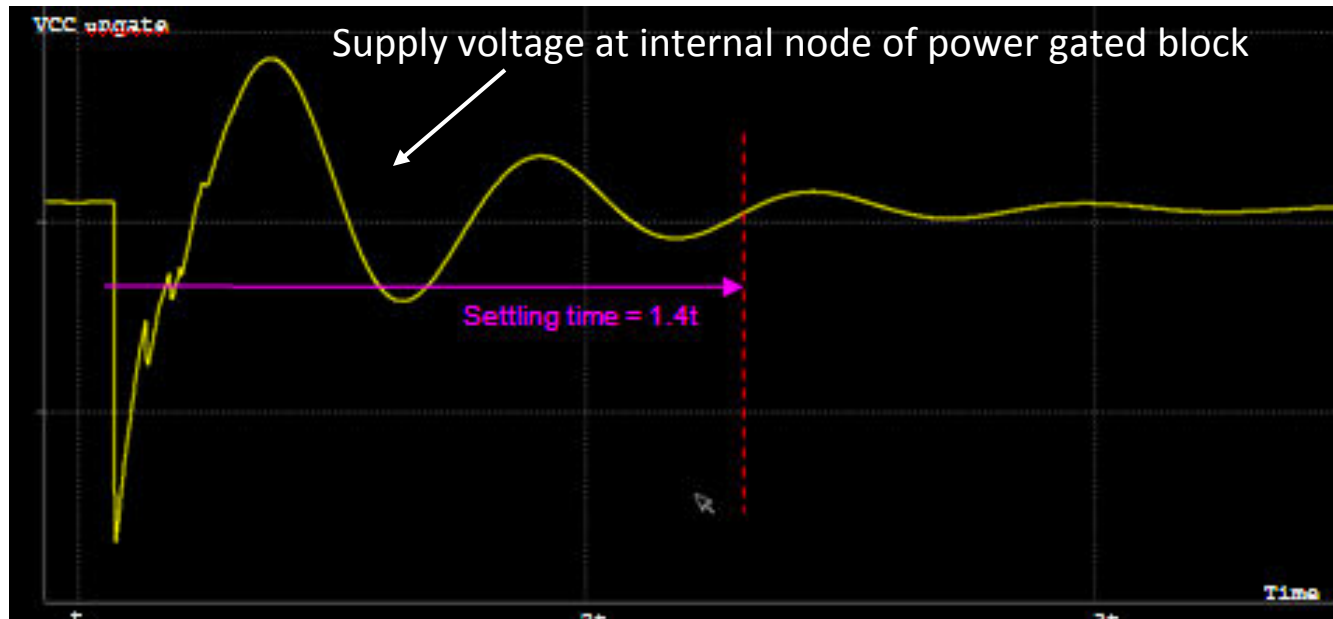
- Off-state standby and on-state operational mode leakage currents monitored
- Closely matched Spice simulation results

# Supply Voltage Settling Time During Power-Up



- Determine time required for voltage to settle down
- Determine appropriate power gate turn-on sequence to reduce voltage fluctuations

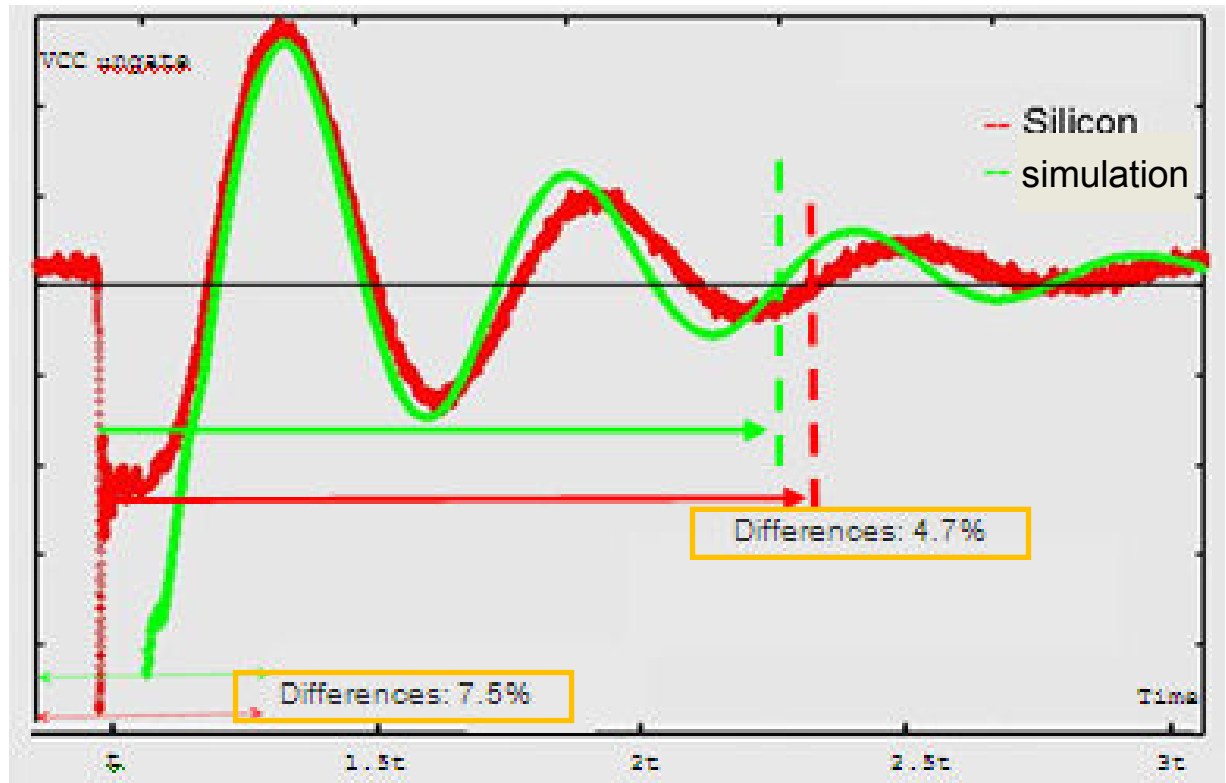
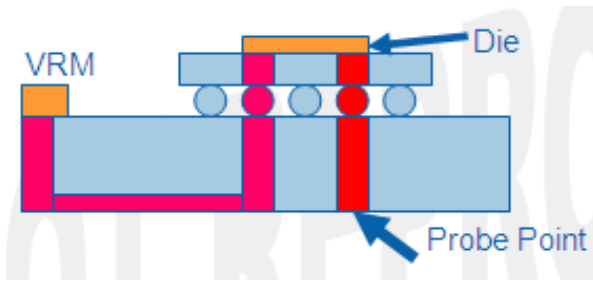
# Optimized Voltage Settling Time During Power-Up



- Reduced voltage settling time by 1/3
- Reduced peak of rush current by 1/3
- Reduced need for on-die and package decaps

# Silicon Measurements

Silicon Measurement Setup



Voltage Swing Comparison between Silicon Measurements and Simulation

# Summary

- **Early design planning through sign-off analyses done for power gated design**
- **Design optimizations done to meet or exceed spec requirements**
- **Silicon correlations performed to match simulations**