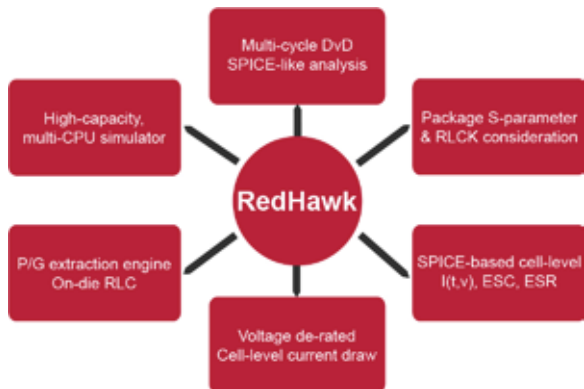


RedHawk-NX

The Next Generation Full-chip Dynamic Power Analysis and Optimization Solution



RedHawk-NX is the next generation full-chip power integrity solution re-architected to meet the capacity and performance requirements of the most advanced designs. RedHawk-NX can be used for early-stage grid prototyping and optimization, pre-tapeout power sign-off, and post silicon debug. It has been silicon-proven with thousands of successful tape-outs by leading semiconductor and fabless semiconductor companies.

Power supply noise consists of resistive network drop (IR drop) and inductive element induced noise (di/dt), which requires a highly accurate full-chip transient simulation solution with a complete picture of the dynamic voltage profile. RedHawk's silicon-proven full-chip dynamic power analysis solution considers resistive, inductive, and capacitive elements from on-die and the IC package grids, the dynamic current drawn by simultaneously switching outputs, and the capacitive loads present in the design. By using RedHawk, engineers can mitigate risks, reduce cost, and improve time-to-market.

Key Capabilities:

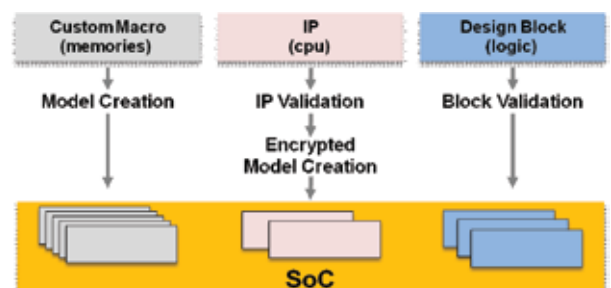
- Single kernel for static IR-drop, Dynamic Voltage Drop (DvD), and EM analysis for ease-of-use and quick time-to-results
- The only hierarchical dynamic (HD) technology for advanced SoC design methodology
- Industry's first Mesh Pattern Recognition (MPR) technology delivering the capacity required to handle hundreds of millions of gates
- Multi-core architecture support leveraging capacity and performance advantages of multiple-CPU computing systems
- Integrated full-chip parasitics extraction of millions of RLC components including self/mutual inductance and 45 degree modeling
- Dynamic library characterization of cell, memory/macro, and I/O with Spice-level accuracy
- Package parasitics impact through integrated RLCK and S-parameter model support
- VCD and Vectorless Dynamic analysis for full-chip coverage
- "What-if" analysis and optimization with built-in GUI and TCL interfaces for real-time layout changes
- Physical design weaknesses identification and automatic noise source repair including wire fixing and decap advisory
- Analysis of dynamic voltage drop impact on timing and jitter
- Chip Power Model (CPM) creation for chip-package-system convergence
- Proven accuracy through correlation with SPICE and measured silicon
- Certified in TSMC and Common Platform Reference Flows

Advanced Design Methodology

RedHawk-NX delivers the industry's first hierarchical dynamic (HD) technology allowing designers to adopt an IP-centric design methodology with various levels of abstraction, while maintaining the sign-off accuracy of a flattened analysis.

RedHawk's hierarchical approach allows creation of models from macros, memories, or sub-blocks that can be used for full-chip top-level simulations. This approach enables a productive and convenient methodology for multi-site design teams by allowing each team to analyze their design sub-blocks and pre-process the analyzed block to create model for use in full-chip simula-

tions. The model creation of Apache's dynamic power views can be performed at various levels of abstraction to allow IP suppliers to control the protection levels of their encrypted IPs.



High Capacity and Performance

RedHawk supports numerous techniques to deliver the highest capacity and performance in full-chip dynamic power analysis. RedHawk's HD technology reduces runtime, peak memory usage, and disk space consumption by 30-50% compared to a full flat analysis, while maintaining accuracy of results. The hierarchical extraction technology, Mesh Pattern Recognition (MPR), reduces memory footprint by 2-3x by utilizing the regularity and patterns in the power grid network. Additionally, with its multi-core support, run-time performance can be reduced as much as 2-3x compared to single thread simulation, especially for MTCMOS rush current analysis.

Sign-off Accuracy

RedHawk full-chip power solution includes integrated high-performance RLC extraction engine, Apache Power Library (APL) pre-characterization, and true-transient simulation. Every cell in the design is pre-characterized using SPICE to model switching current waveforms and RC parasitics for different input slew, output load, supply voltage, and operating states. Its simulation engine considers all necessary capacitive elements and associated resistive components, as well as the package and board models in S-parameter or RLCK format.



Typically, RedHawk's transient simulation results are within 2% of SPICE and measured silicon.

VCD and Vectorless Dynamic

RedHawk supports both RTL and gate-level VCD vectors. For RTL vectors, RedHawk uses "state propagation" engine to derive the toggle activity and "cycle selection" technology to identify the relevant clock periods based on criteria such as power consumption, power variation, impact on DvD, frequency, etc.

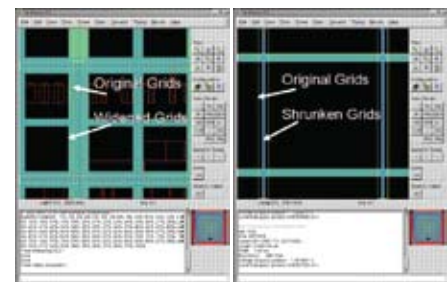
RedHawk's Vectorless Dynamic engine generates cycle by cycle switching scenario based on user specified constraints such as power consumption, design and cell logic properties, etc. With the Vectorless engine designers can accurately analyze the impact of package parasitics, on-chip inductance, and decaps on transient "hot spots", without user provided stimulus inputs.

Connectivity Verification and Weakness Exploration

RedHawk can verify power/ground connectivity issues such as shorts, opens, missing vias and other weaknesses. Its network topology analysis provides insights into routing issues that can cause voltage drop hot-spots or current congestions in the design. The current flow from voltage supply pads to every cell or transistor is provided as an overlay on the design layout allowing one to identify cases where the "shortest" path is not being taken. With RedHawk's debug and analysis features, designers can isolate design weaknesses and identify their causes.

Design Repair with 'What-If' and FAO

RedHawk supports extensive "what-if" capabilities for power-grid exploration and design trade-off assessments. A layout driven, incremental "what-if" analysis enables designers to explore design fix scenarios with rapid turn-around time. SoC designers can assess design trade-off, such as package RLC effects, and accurately determine the most effective decap insertion scheme. Designers can also explore ways to reduce IR drop and EM violations by adding, deleting or editing power/ground pads, power straps and vias or via arrays.



RedHawk with optional FAO automatically optimizes decaps to reduce the peak IR-drop and eliminate ineffective decap cells that can impact leakage and yield. FAO can be used to re-design the power grid mesh without compromising the total voltage drop.

Design Prototyping

RedHawk supports early-stage power grid prototyping through extensive set of layout drawing commands, or by reading in partial design information such as initial floorplan placement of the blocks along with their power consumption. During prototyping, RedHawk can guide pad/bump placements, identify current congestion areas, and direct power-gate design and placement. From the prototype analysis, Chip Power Model (CPM), an early models of the die can be generated, allowing package and board designers to determine the number of layers needed in the package, the pin count, and the routing and via placement needs.

Apache Design Solutions

2645 Zanker Road
San Jose, CA 95134
www.apache-da.com