

Full-chip Vectorless Dynamic Power Integrity Analysis and Verification Against 100uV/100ps-Resolution Measurement

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Abstract

The advances in semiconductor manufacturing, EDA tools, and VLSI design technologies are enabling circuit designs with increasingly higher speed and density. However, this trend is causing on-chip power distribution network to experience larger dynamic voltage fluctuations due to dynamic voltage drop, L di/dt noise, and/or LC resonance. As a result, the analysis of power-integrity, as well as the evaluation and calibration of the analysis methodology, has become a major challenge in designing high-performance circuits. An innovative vectorless dynamic power-ground noise analysis approach is discussed in this paper. This approach addresses full-chip complexity with transistor-level accuracy. This analysis approach demonstrated very good correlation with an on-chip supply noise measurement in 0.13-um CMOS technology, capable of achieving 100uV/100ps resolution.

1. Introduction

Circuits with increasingly higher speed and density are causing significant on-chip power-ground voltage fluctuations due to dynamic voltage drop, L di/dt noise, and/or LC resonance. Assuming constant field scaling, the percentage of di/dt to Vdd scales as S^4 , when process is scaled by 1/S [1]. On the other hand, process scaling imposes power supply voltage (Vdd) reduction which has also been decreased to aggressively save power consumption. As a result, power-ground integrity has become one of the most critical issues as designs transition to 130nm and 90nm process technologies. For example, a 10% supply voltage fluctuation can translate to more than a 15% timing uncertainty and may even cause the circuit to fail. In addition, power-gating is often employed to reduce leakage power, which causes sudden change in current and significant increase L di/dt noise when a gated block is turned on. Also, inductance may resonate with intrinsic and incorrectly inserted de-coupling capacitors.

Existing static IR-drop signoff methodology, based on “average” power [2] and conservative over-designing of the power grid have become inadequate to protect designs from supply-noise induced logic and timing failures. Static IR analysis is unable to consider the following’s impact on timing.

1. Simultaneous Switching Outputs (SSO) in core, memory/IP, and I/O regions.
2. On-chip or packaging inductance and their coupling.
3. Intrinsic and intentional decoupling capacitance.

Furthermore, to control dynamic power noise, circuit designers rely on the transient analysis that can tell the effectiveness of their inserted decoupling capacitors. Due to RC delay, decoupling capacitors placed far away from the hot spots do not decrease supply noise and only consumes leakage power.

The complexity of dynamic power verification is enormous since it involves full-chip transient simulation of a tightly interconnected power network, transistors’ nonlinear parameters, and packaging parasitics. The switching characteristics are time and logic dependent, which implies that extensive vectors and long simulation run are required. But due to the capacity, performance, and accuracy limitations of existing SPICE or fast-SPICE-based solutions, a stimulus-driven approach can only be applied to small blocks of a design. And even after simulating millions of vectors, designers still have no idea of how close they are to finding the worst case vector. A proposal was made by researchers to apply ATPG technology to search for peak-noise input vector [3]. However, this approach did not consider the RLC parasitics of the power network, which can greatly influence the amount of noise.

To avoid reliance on finding the peak-noise vector, we present in this paper, a full-chip *vectorless* dynamic power integrity analysis approach. It performs a full-chip transient simulation, considering effects of all inductors and capacitors, while statistically determining the peak-

noise switching scenario without the need for input vectors. It is able to provide cell-level complexity while achieving transistor-level accuracy through SPICE pre-characterization of switching current profile, transistor intrinsic parasitics, and cell delay impacts from dynamic voltage drops. This approach is discussed in Section 2.

To verify our analysis result, we built a test chip implementing an on-chip supply and well noise detector in 0.13 μ m, 1.5V CMOS technology [4]. The detector is able to achieve 100 μ V/100ps resolution, providing the ability to monitor dynamic supply noise waveform for the first time. We measured Vdd noises at a 200MHz register file of a product processor and SRAM operating at 100MHz and 200MHz. The vectorless dynamic analysis results were verified against these waveforms with very good correlation. The measurement setup will be introduced in Section 3 and the comparison results will be given in Section 4.

2. Statistical Vectorless Dynamic Power Supply Analysis

To achieve transistor-level accuracy, our vectorless dynamic analysis, whose flow is shown in Figure 1, is composed of three processes: (1) switching scenario creation, (2) RLC parasitic extraction, and (3) current-profile characterization and transient simulation. They are discussed in subsequent sections.

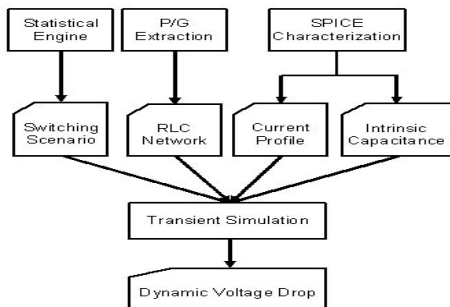


Figure 1. Vectorless Dynamic P/G noise analysis flow.

2.1. Switching Scenario Creation

A peak-noise switching scenario comprises three parts: (1) which instance will switch, (2) how they will switch (0-> 1 or 1->0), and (3) when they will switch. The possible switching timing window of each instance is determined based on the Static Timing Analysis (STA). Which instance will switch, how they will switch, and when they will switch within that timing window is determined statistically. Characteristics considered in the scenario creation include:

1. **Toggle probability of each instance.** An instance with larger toggling probability is likely to toggle in the worst case. This probability may be derived from logic simulation of representative input

streams or from probability propagation as in [6].

2. **Switching energy of each instance.** In the worst case, high power instances, such as bus drivers are more likely to toggle so their toggling probabilities are scaled higher by the switching energy.

3. **Peak cycle power.** Designers need to provide peak cycle power as a constraint for the scenario. Based on previous designs or by scanning each cycle powers of representative input streams, designers may have the knowledge of the “peak cycle power” over the “average power” ratio, defined as **PAR**. Since the chip’s average power is easier to estimate, the peak cycle power may be derived by multiplying the average power with PAR.

4. **Instance logic function.** Based on the toggling probability and the peak cycle-power constraint, “which instance to toggle” and “how to toggle” may be assigned statistically. However, there may be logic conflicts among the assignments. Because it is almost impossible to resolve conflicts completely, it is resolved locally in the logic network by keeping the assignment of high power instances and changing the assignment of low power instances to meet the logic requirement.

2.2. RLC Parasitic Extraction

The on-chip power-grid R and L extraction is performed based on the Partial Element Equivalent Circuit (PEEC) method [7]. Since the coupling of the partial inductance given from PEEC extends to long range, the L matrix may be large and dense. To make the L matrix sparse, we employ the approach of “Quick On-Chip Self- and Mutual-Inductance Screen” [8] for inductance screening.

The on-chip decoupling capacitance (decap) is composed of five components:

1. **Intrinsic device decoupling capacitance inside a cell, including built-in decoupling protection.** SPICE AC analysis is used to determine the impedance between Vdd and Vss pins at the chip’s dominant operating frequency. The decap and effective series resistance (ESR) can be derived from the imaginary and the real part of the impedance, respectively.

2. **Decoupling loading capacitance.**

For an instance with its output at high, there is a conducting path from the instance’s Vdd pin through one or more PMOS to the grounded loading capacitance, which is connected to the instance’s output pin. This load capacitance acts as decoupling capacitance and should be considered in the simulation.

3. **Inserted decoupling capacitors.** The value is also extracted through SPICE AC analysis.

4. **Coupling capacitance between Power and Ground wires.** The Two-and-half-D Capacitance

Extraction [9] approach is employed to determine this coupling capacitance. In general, this capacitance only contributes to several percentages of the total decoupling capacitance.

5. **Well capacitance.** The junction capacitance of P- or N-well need to be considered as they form a significant portion of cell's intrinsic decap. The value is either based on the well's geometry and the capacitance density provided by process foundry, or modeled as diodes in the SPICE deck by the library vendors and extracted from SPICE AC analysis.

2.3. Current Profile Characterization and Transient Simulation

To achieve cell-level complexity and transistor-level accuracy, SPICE transient simulation is used to characterize the supply current profile of each instance, in addition to characterizing intrinsic decap discussed above. The distributed RC parasitics of signal wires are extracted by a commercial tool and reduced to C1-R-C2 pie model by using AWE [10]. The input slew information is given from STA.

SPICE transient simulation of the cell connected to its C1-R-C2 and having the input slew at different Vdd supplies are performed to extract the current profiles, which is saved for full-chip simulation run. Since multiple instances of the same cell may have similar C1-R-C2 and slew, the number of characterizing simulations may be reduced by clustering similar samples, resulting in design dependent pre-characterization of a 10-million gate design to finish within a day.

With the characterizations above, the transistor-level circuit is transformed into a linear circuit with P/G RLC. Then a full-chip simulation is performed in order to consider the packaging and inductive coupling effect. The simulation result will show the effectiveness of decoupling capacitance, LC resonance, and most importantly, the weakness of the P/G grid.

3. Dynamic Supply Noise Measurement

Dynamic supply noise probing has been difficult due to the in-negligible impedance of the probe tip changing the noise waveform, and the attenuation through the probe limiting the resolution. The fast edge of the noise is difficult to capture, and therefore, the most feasible method for measuring dynamic supply noise is by using on-chip measuring devices.

The application of waveform-accurate measurement technology developed to measure the substrate noise [4] has been extended to measure the power-supply and well noise [5], where the high resolution noise detectors are arrayed and multiple points within a circuit under test (CUT) was probed, as shown in Figure 2.

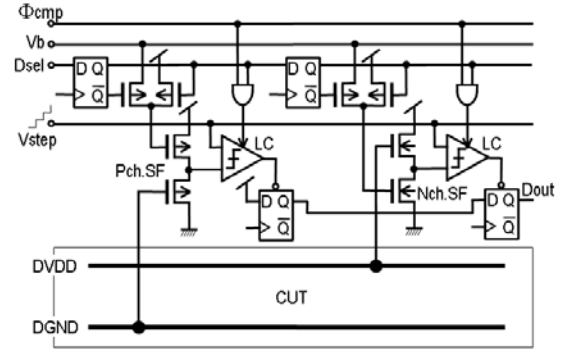


Figure 2. High-resolution on-chip noise detectors.

The noise detector consists of a source follower (SF), latch comparator (LC), and circuitry for selective activation. The SF senses voltages at measurement points and the output is sampled and digitized on chip using the LC. However, to measure noise with good dynamic range and high resolution, without being dependent on clock frequency, a system that gives sample timing and reference voltage from off-chip was used. This method resulted in waveform noise measurement that can handle hundreds of nanoseconds of measuring time, with a large dynamic range of 2V, attained with high precision of 100uV/100ps.

4. Result and Comparison

Figure 3 shows the die photo of a 200MHz product processor as CUT with the measurement device. The chip size is 5.4mm x 5.4mm with 6 layers of metal. The power-supply and ground domains are isolated by triple wells. In addition, with the exception of logic circuit that is based on standard logic cell, the source and body terminals of both N-well and P-well are separately wired to enable forward biasing. The ground lines and P-substrate are combined together within the chip to provide a common reference voltage.

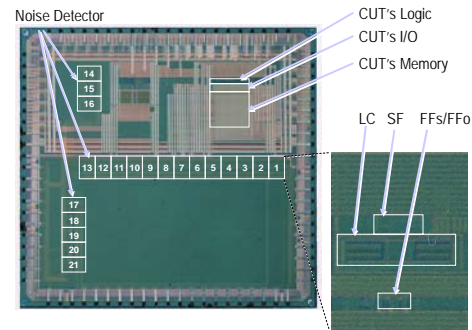


Figure 3. Die photo.

We measured the Vdd rail noise at locations shown in the figure when the processor is executing Register mode and SRAM mode. The measured noise waveform is

recorded. Separately, a vectorless dynamic analysis of the whole chip is performed and the V_{dd} waveforms for the same locations are generated. In order to validate our vectorless approach, the waveforms at these modes are compared. The PAR constraint of the analysis is set by scanning the cycle powers from gate-level logic simulation of 80 representative clock cycles. The PAR is equal to the peak cycle power of those cycles divided by their average power.

The total vectorless analysis took 5 minutes CPU time and 700MB peak-memory on a 3.2GHz Pentium4 Linux PC. The CPU and memory include design parsing, on-chip RLC extraction, and full-chip transient simulation.

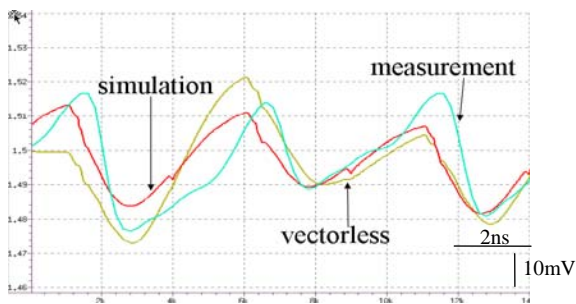


Figure 4. 200MHz Register mode waveform comparison.

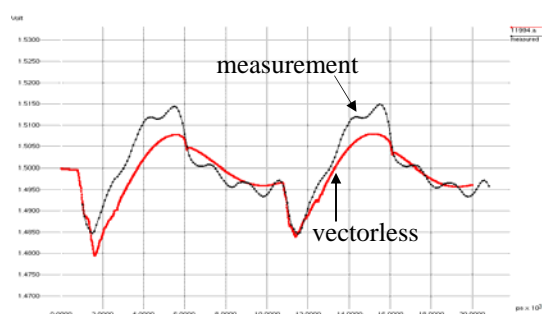


Figure 5. SRAM mode waveform at 100 MHz comparison.

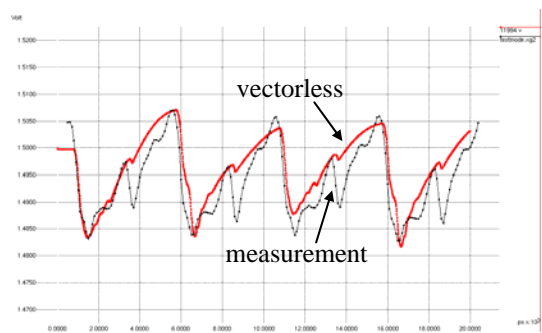


Figure 6. SRAM mode waveform at 200 MHz comparison.

Figure 4 shows the waveform comparison between the vectorless dynamic analysis and the silicon measurement during Register mode. Input stimuli-driven simulation waveform is also included in the comparison. Figures 5 and 6 show the waveform comparisons at 100MHz and

200MHz SRAM modes, respectively. Because vectorless analysis is used to verify the worst case, emphasis should be addressed to the difference at the peak noise. Only 8mV maximum voltage difference (about 12% of the peak-to-peak swing) is observed, demonstrating good correlation and accuracy of vectorless dynamic analysis approach. Also, measurement of 100uV/100ps resolution was achieved from the edge rate of the waveform.

5. Conclusions

A full-chip transient simulation is required to determine the impact of chip package, on-chip/off-chip inductance, decoupling capacitance, and core and IO SSO, to the dynamic power-ground noise. From the noise waveform, along with each instance's switching timing window, the impact to timing can be analyzed. Previous methods required transient simulations that relied on users' input vectors. However, for peak supply noise analysis, it is almost impossible to find an input stream that covers all operational corners, and to simulate that long input stream.

In this paper, we have presented a statistical vectorless dynamic supply noise analysis, which performs transient simulation without users' input vectors. To verify the accuracy of this approach, an on-chip supply noise measurement apparatus, which is able to achieve 100uV/100ps resolution, was used. From the comparison against the measurement, the accuracy of the vectorless dynamic analysis approach was proven.

6. References

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