

# Your Analysis Partner for Chip-Package-System Convergence



Issue No. 4 - January 2009

## Apache Spotlight

### RedHawk-NX

#### **The Next Generation Full-chip Dynamic Power Integrity Solution**

RedHawk-NX is the next generation dynamic power integrity solution re-architected to handle designs of five hundred million gates, while maintaining sign-off accuracy. The advanced technologies in RedHawk-NX include:

- **HD:** The industry's first **Hierarchical Dynamic** technology for power analysis
- **MPR:** Proprietary **Mesh Pattern Recognition** algorithm for 2-3x memory footprint reduction and reuse
- **MC: Multi-core** architecture support for maximizing the capacity and performance advantages of multi-processor machines

RedHawk-NX supports the industry's first hierarchical dynamic technology allowing designers to adopt a bottom-up analysis methodology with various levels of abstraction. With HD technology, IP providers can deliver encrypted Apache dynamic power views for use in full-chip sign-off analysis. When using HD's 'white-box' mode, the designers are able to maintain the same level of sign-off accuracy as RedHawk's flattened analysis.

RedHawk-NX's automatic mesh pattern recognition algorithm leverages regularity in the power/ground mesh structures enabling data reuse for effective reduction of physical memory needs. MPR handles designs with complex RDL, dense multi-layered P/G grid, and high memory content.

RedHawk-NX is re-architected to maximize the capacity and performance advantages of the multi-core processing systems. The MC solver can be scaled to handle designs with up to billion nodes in existing computing environment. With the MC technology, designers will benefit from 2-3X runtime improvements in their dynamic transient simulation, as well as MTCMOS rush current analysis.

[More on RedHawk-NX >>>](#)

[Redhawk-NX Press Release >>>](#)

## Articles

[Chip/package/PCB co-simulation – what it is, why it's needed - SCDsource](#)

### Power Noise Analysis for Next Generation ICs



*This paper describes the challenges associated with power delivery network designs and how a full-chip dynamic power analysis tool addresses design failures caused by dynamic power noise. It details the capabilities of Apache's flagship power integrity solution, RedHawk, including the latest NX technologies.*

[Request Download](#)

## Whitepapers

- Power Noise Analysis for Next Generation ICs

## Visit Apache at DesignCon 2009

### DesignCon 2009

Santa Clara Convention Center  
February 3-4, 2009  
Booth #514

### Booth Demonstrations

**PakSi-E** Learn how PakSi-E's 3D FEM electromagnetic extraction, modeling, and analysis capabilities enable IC package and system-in-package (SiP) designers to perform highly accurate power integrity, signal integrity, and simultaneous switching noise (SSN) analysis.

**Chip Power Model (CPM)** Learn how CPM allows package/SiP/PCB designers to perform better noise budgeting, predict global power delivery network target impedance and resonance, and optimize package/SiP/PCB designs from early in the design process for cost reduction and risk mitigation.

**Sentinel-PI** Learn how Sentinel-PI's 3D full-wave power network extraction and power integrity engine, along with seamlessly integrated CPM, provide the most accurate "IC-aware" modeling and analysis of the system-level power delivery network, enabling IC package, System-in-Package (SiP), and PCB designers to optimize their design from early prototyping to sign-off.

**Sentinel-SSO** Learn how Sentinel-SSO enables designers to better assess the SSO impact on timing and optimize I/O pad selections and placements for efficient power/ground to signal pad ratios, and resolve system timing closure issues in high-speed parallel interfaces.

### Conference Sessions

#### **Worst-Case Switching Pattern for Core Noise Analysis (4-TA3)**

**When:** Tuesday, February 3, 10:15AM to 10:55AM

**Where:** Ballroom J

*This paper demonstrates an optimum methodology to capture the worst-case switching activity when performing the power integrity analysis for the core power of ASIC. [More >>>](#)*

#### **Collaboration Across the Changing Design Chain**

**When:** Tuesday, February 3, 2:00PM to 3:30PM

**Where:** Room 203/204

*This panel will discuss the challenges faced by IC and system designers on reaping the benefits of SiP technology and what foundries and package providers are doing to make SiP a reality. [More >>>](#)*

#### **Multi-Die Chip/Package Co-Design for SiP Applications**

**When:** Tuesday, February 3, 3:45PM to 5:00PM

**Where:** Ballroom G

*This panel will discuss the challenges faced by the IC and package teams as power, SI, reliability, thermal, stress, etc. issues further exacerbates design and validation of multi-die chips, and the solutions needed to address these challenges. [More >>>](#)*

- Power Closure Flow
- Leakage Analysis
- Jitter Noise Analysis
- Power Thermal Analysis

[Click here](#) to register and download whitepapers.

---

## Recent News

- [Apache Introduces RedHawk-NX, the Next Generation Full-chip Dynamic Power Integrity Solution](#)
- [Apache Ranks in Top 15 of the Fastest Growing Software and Information Technology \(IT\) Companies in Deloitte's Technology Fast 50](#)
- [Apache Design Solutions Achieves Record Sales for the Twenty-Third Consecutive Quarters](#)
- [Apache upgrades RedHawk for full-chip power integrity - \*\*SCDsource\*\*](#)
- [The New RedHawk NX Power Integrity Analysis - \*\*EDACafe\*\*](#)

## Upcoming Events



**SNUG 2009**  
San Jose, CA  
March 17,2009



**DATE 2009**  
Nice, France  
April 20 - 24

---

## Customer Support

[Apache's online support center](#) is now available for existing customers.

[Click here](#) to register

---

## To Subscribe

[Click here](#) to subscribe to future issues of News from Apache Design Solution.

### Privacy Notice

Apache Design Solutions respects your online time and internet privacy. If you prefer not to receive future notifications, please forward this message to [unsubscribe](#) and you will be removed from the list.