

Your Analysis Partner for Chip-Package-System Convergence



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Apache Spotlight

Totem

The Industry's First Power and Noise Integrity Platform for Analog and Mixed-Signal Designs

Totem is a Power-Noise-Reliability platform for analog, mixed-signal, memory, and high-speed I/O designs. It enables designers to account for the impact associated with global coupling of power/ground noise, substrate noise, and package/PCB capacitive and inductive noise on their designs.

- **Totem-MMX:** A transistor-level IR/dynamic voltage drop analysis solution for power/ground network at the IP and the full-chip level. It also supports IP model generation and signal EM validation.
- **Totem-SE:** A full-chip solution for modeling and simulating the substrate noise injection and coupling through the on-die power/ground network.

[More on Totem >>>](#)

[Totem Press Release >>>](#)

[Totem Whitepaper >>>](#)

RedHawk, Sentinel, and Totem Eco-Platform

A Chip-Package-System Convergence Solution for Cost Reduction and Risk Mitigation

Apache's power and noise integrity eco-platform for chip-package-system convergence includes RedHawk SoC, Totem analog and mixed signal, and Sentinel package/PCB platforms. The eco-platform addresses the unique challenges associated with each design domain while providing an integrated flow for digital, custom IP, and System worlds.

Apache's model-based convergence platform enables SoC designers to consider the impact of analog noise by importing an accurate and efficient Component Macro Model (CMM) generated by Totem and S-parameter model representing the package and PCB parasitics from Sentinel into RedHawk SoC analysis. The Analog IP designers can see the effects of digital core noise injection into its shared substrate and the IC package, PCB, and SiP designers can import widely adopted Chip Power Model (CPM) to analyze the impact of on-die noise. Apache's eco-platform allows each designer to stay within their native environment while obtaining valuable data that can ensure performance and accuracy of their design.

Articles/Interviews

- **Demos on Demand** - [Richard Goering and Andrew Yang discuss the industry, business model and Apache's strategy](#)
- **EDN** - [Totem offers full-chip power and noise integrity analysis for chips with analog content](#)
- **EDN** - [Apache's RedHawk included in TSMC sign-off flows](#)
- **PCBDesign007** - [Andrew Yang shares Apache's role in power and signal integrity of package and PCB designs](#)
- **EDA Cafe** - [Aveek Sarkar talks about Apache's power and noise analysis platforms](#)

Recent News

- [RedHawk Certified to Support TSMC's iRCX Format](#)

Techguri Blog

The New Peer-to-Peer, Geek-to-Geek "Technology Focused" Blog

Meet Apache's Techguri Blog authors and read their informative technical posts on topics covering Low Power, Analog Design, IC/Package/SiP and more!

Aveek Sarkar a Vice President of Product Engineering and Support works closely with customers to address their power and noise challenges.

"We had just announced Totem™, our full-chip transistor level power noise and reliability analysis solution which many of our users in Israel have been using for some time. We were seeing increased acceptance of our co-design methodology ... and many of our Israel customers had provided important feedbacks in defining this methodology." [MORE](#)

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[Low Power](#)

Upcoming Events



TSMC Symposium
June 18 - Hsin Chu,
Taiwan
June 25 - Shanghai, China



DAC 2009
San Francisco, CA
July 27 - 30, 2009
Booth #722



EMC Austin
Austin, TX
August 18 - 20, 2009

Whitepapers

- Power and Noise Integrity for Analog/Mixed-Signal Design
- Power Noise Analysis for Next Generation ICs
- Power Closure Flow
- Low power Design Analysis
- Jitter and Critical path Timing Analysis

[Click here](#) to register and download whitepapers.

Customer Support

- [RedHawk Power Integrity Solution Adopted by AppliedMicro for their SoC and Mixed-Signal Designs](#)
- [Apache Introduces Totem, the Industry's First Power and Noise Integrity Platform for Analog and Mixed-Signal Designs](#)
- [NEC Adopts Apache's Dynamic Power Sign-off Solution for SoC Designs](#)
- [Apache and NXP Collaborate to Address 45nm Power Integrity Challenges for Advanced Digital Processor Design](#)
- [Apache Deepens Collaboration with ST to Address Power and Noise Challenges for 45/32nm Designs](#)

[Apache's online support center](#) is available for existing customers.
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